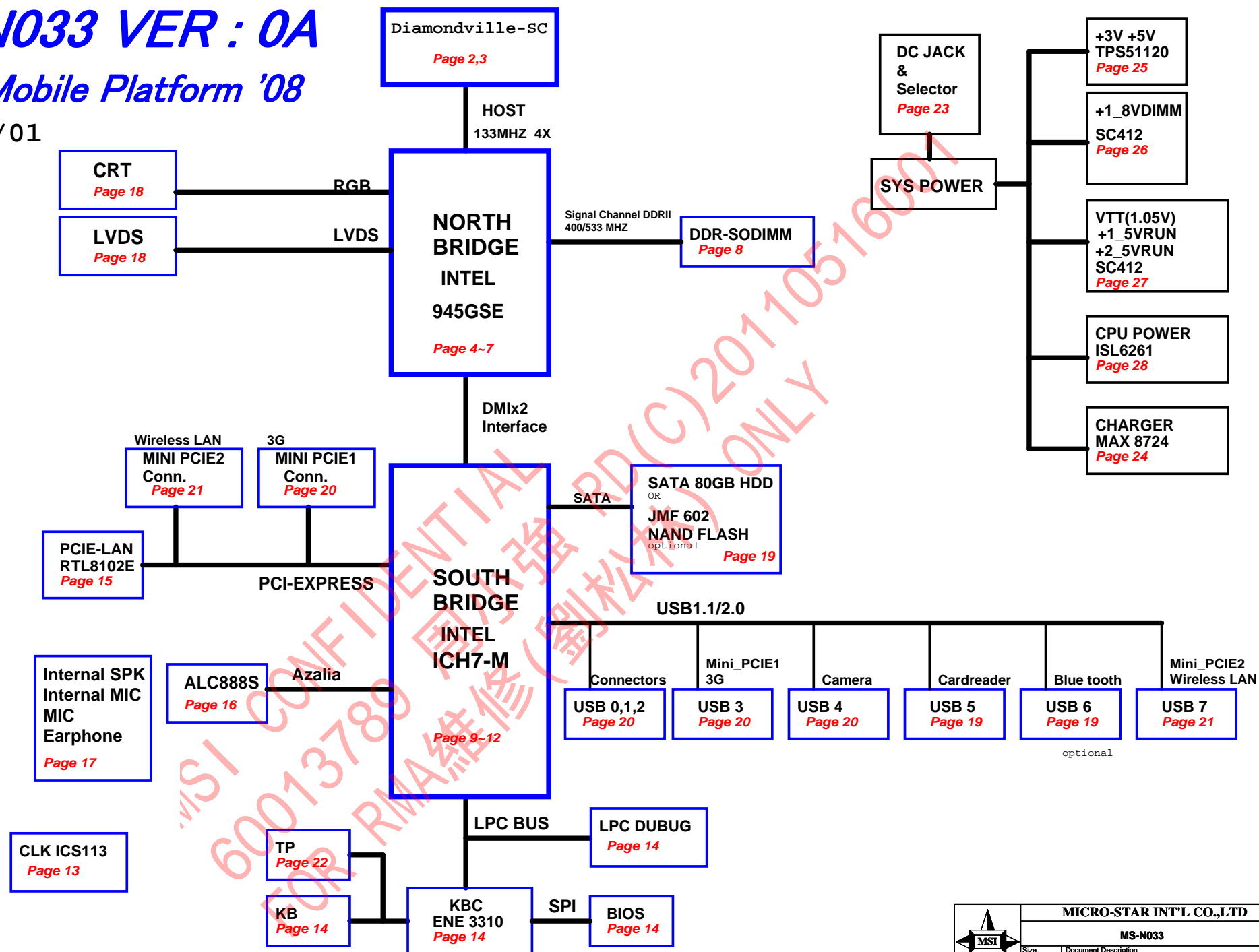
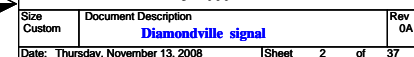


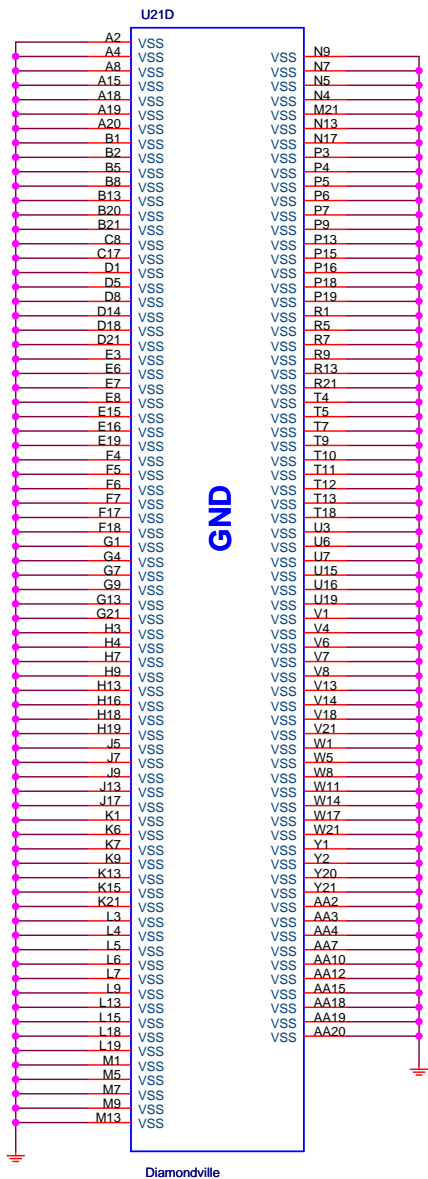
MS-N033 VER : 0A

Basic Mobile Platform '08

2008/10/01

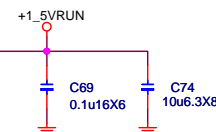
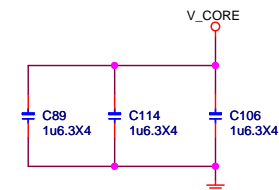
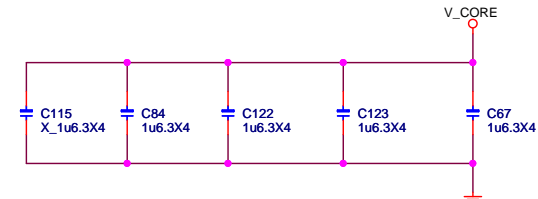
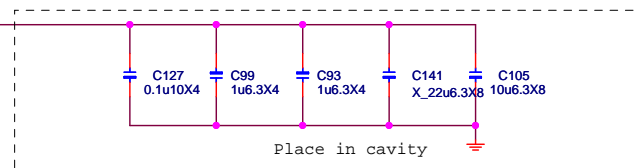
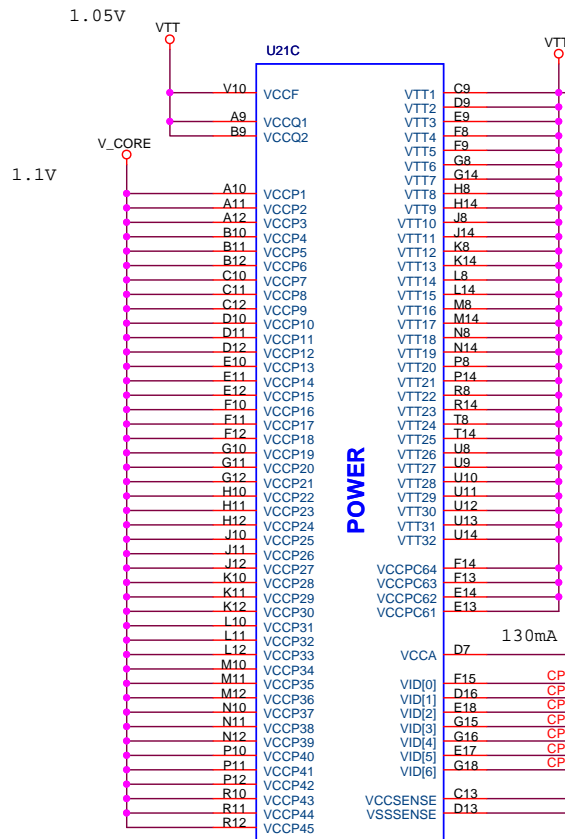




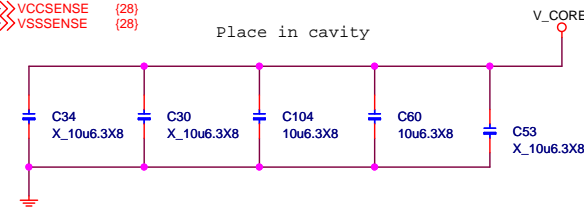
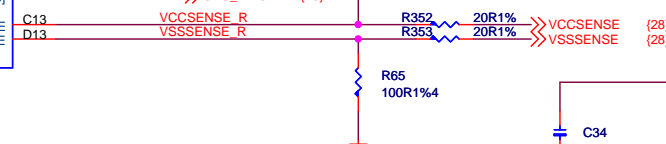


2.5A: before VCC stable
1.5A: after VCC stable

LAYOUT NOTE:
Route VCCSENSE and VSSSENSE
traces at 27.4Ohms with 50
mil spacing.
Place PU and PD within 1
inch of CPU.



130mA



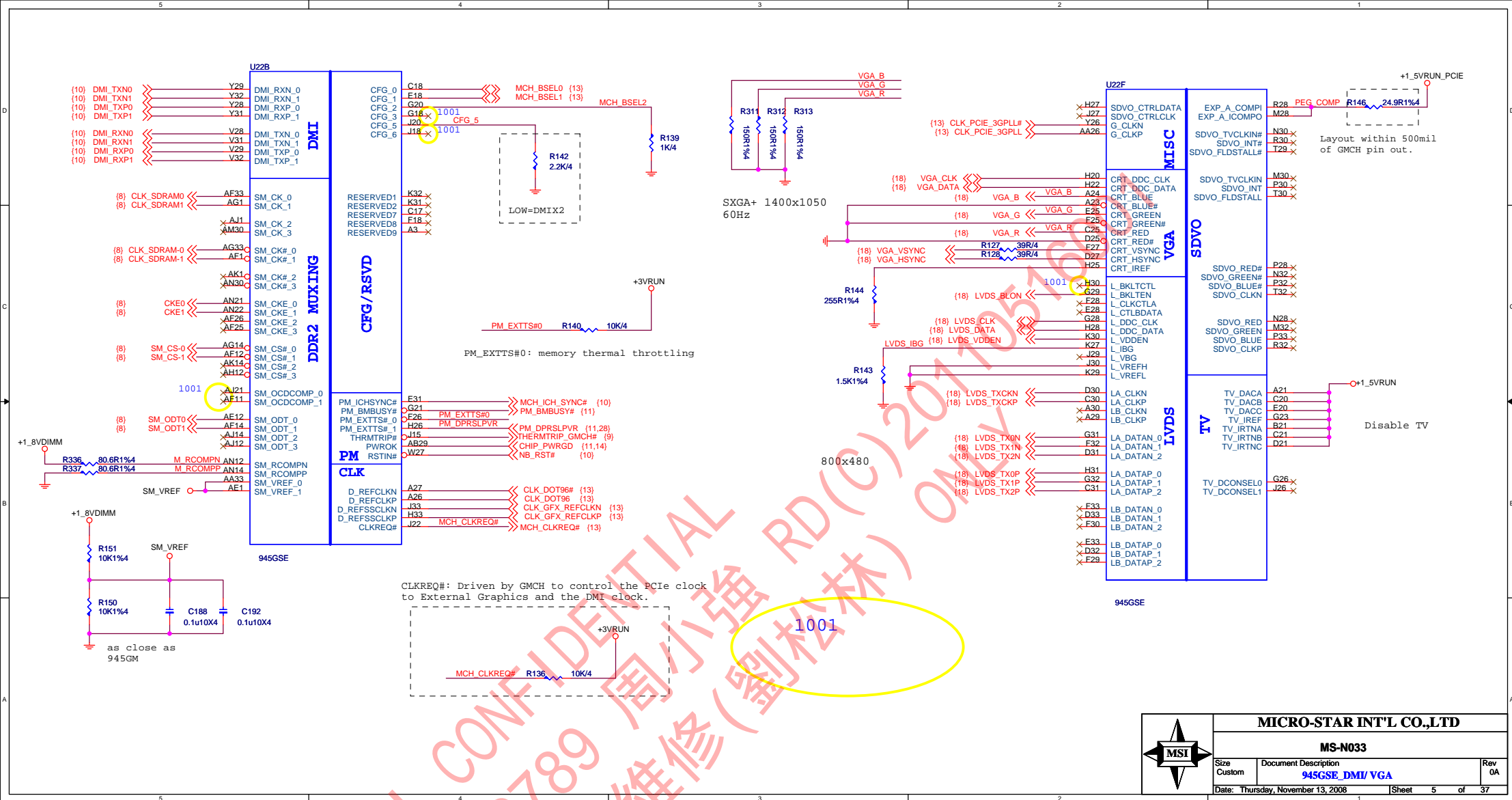
close to cpu socket



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MS-N033

Size	Document Description	Rev
Custom	Diamondville Pown/GND	0A
Date: Thursday, November 13, 2008	Sheet 3 of 37	



(8) SA_MD[0..63] <<>

U22C

SA MD0	AC31	SA DO_0
SA MD1	AB28	SA DO_1
SA MD2	AE33	SA DO_2
SA MD3	AF32	SA DO_3
SA MD4	AC33	SA DO_4
SA MD5	AB32	SA DO_5
SA MD6	AB31	SA DO_6
SA MD7	AE31	SA DO_7
SA MD8	AH31	SA DO_8
SA MD9	AK31	SA DO_9
SA MD10	AL28	SA DO_10
SA MD11	AK27	SA DO_11
SA MD12	AH30	SA DO_12
SA MD13	AL32	SA DO_13
SA MD14	AJ28	SA DO_14
SA MD15	AJ27	SA DO_15
SA MD16	AH32	SA DO_16
SA MD17	AE31	SA DO_17
SA MD18	AH27	SA DO_18
SA MD19	AF28	SA DO_19
SA MD20	AJ32	SA DO_20
SA MD21	AG31	SA DO_21
SA MD22	AG28	SA DO_22
SA MD23	AG27	SA DO_23
SA MD24	AN27	SA DO_24
SA MD25	AM26	SA DO_25
SA MD26	AJ26	SA DO_26
SA MD27	AJ25	SA DO_27
SA MD28	AL27	SA DO_28
SA MD29	AN26	SA DO_29
SA MD30	AH25	SA DO_30
SA MD31	AG26	SA DO_31
SA MD32	AM12	SA DO_32
SA MD33	AL11	SA DO_33
SA MD34	AH9	SA DO_34
SA MD35	AK9	SA DO_35
SA MD36	AM11	SA DO_36
SA MD37	AK11	SA DO_37
SA MD38	AM8	SA DO_38
SA MD39	AK8	SA DO_39
SA MD40	AG9	SA DO_40
SA MD41	AF9	SA DO_41
SA MD42	AF8	SA DO_42
SA MD43	AK6	SA DO_43
SA MD44	AE7	SA DO_44
SA MD45	AG11	SA DO_45
SA MD46	AJ6	SA DO_46
SA MD47	AH6	SA DO_47
SA MD48	AM6	SA DO_48
SA MD49	AK3	SA DO_49
SA MD50	AL2	SA DO_50
SA MD51	AM5	SA DO_51
SA MD52	AL5	SA DO_52
SA MD53	AJ3	SA DO_53
SA MD54	AJ2	SA DO_54
SA MD55	AG2	SA DO_55
SA MD56	AE3	SA DO_56
SA MD57	AE7	SA DO_57
SA MD58	AF6	SA DO_58
SA MD59	AH5	SA DO_59
SA MD60	AG3	SA DO_60
SA MD61	AG3	SA DO_61
SA MD62	AF5	SA DO_62
SA MD63	AF5	SA DO_63

AG19# SB_CAS#
AG21# SB_RAS#
AG20# SB_WE#

945GSE

DDR2 SYSTEM MEMORY

SA_BS_0	AK12	SA_BS-0
SA_BS_1	AH11	SA_BS-1
SA_BS_2	AG17	SA_BS-2
SA_DM_0	AB30	SA_DM0
SA_DM_1	AL31	SA_DM1
SA_DM_2	AF30	SA_DM2
SA_DM_3	AK26	SA_DM3
SA_DM_4	AL3	SA_DM4
SA_DM_5	AG7	SA_DM5
SA_DM_6	AK5	SA_DM6
SA_DM_7	AH3	SA_DM7
SA_DQS_0	AC28	SA_DQS0
SA_DQS_1	AJ30	SA_DQS1
SA_DQS_2	AK33	SA_DQS2
SA_DQS_3	AL25	SA_DQS3
SA_DQS_4	AN9	SA_DQS4
SA_DQS_5	AH8	SA_DQS5
SA_DQS_6	AM2	SA_DQS6
SA_DQS_7	AE3	SA_DQS7
SA_DQS#_0	AC29	SA_DQS#_0
SA_DQS#_1	AK30	SA_DQS#_1
SA_DQS#_2	AJ33	SA_DQS#_2
SA_DQS#_3	AM25	SA_DQS#_3
SA_DQS#_4	AN8	SA_DQS#_4
SA_DQS#_5	AJ8	SA_DQS#_5
SA_DQS#_6	AM3	SA_DQS#_6
SA_DQS#_7	AE2	SA_DQS#_7
SA_MA_0	AJ15	SA_MA0
SA_MA_1	AM17	SA_MA1
SA_MA_2	AM15	SA_MA2
SA_MA_3	AH15	SA_MA3
SA_MA_4	AK15	SA_MA4
SA_MA_5	AN15	SA_MA5
SA_MA_6	AJ18	SA_MA6
SA_MA_7	AF19	SA_MA7
SA_MA_8	AN17	SA_MA8
SA_MA_9	AL17	SA_MA9
SA_MA_10	AG16	SA_MA10
SA_MA_11	AL18	SA_MA11
SA_MA_12	AG18	SA_MA12
SA_MA_13	AL14	SA_MA13
SA_CAS#	AJ17	SA_CAS#
SA_RAS#	AK18	SA_RAS#
SA_WE#	AN28	SA_WE#
SA_RCVENIN#	AM28	SA_WE#
SA_RCVENOUT#	AH17	SA_WE#
SB_BS_0	AH21	SA_BS-0
SB_BS_1	AJ20	SA_BS-1
SB_BS_2	AE21	SA_BS-2
SB_MA_0	AN29	SA_MA0
SB_MA_1	AL24	SA_MA1
SB_MA_2	AK21	SA_MA2
SB_MA_3	AK22	SA_MA3
SB_MA_4	AL26	SA_MA4
SB_MA_5	AG22	SA_MA5
SB_MA_6	AE21	SA_MA6
SB_MA_7	AE21	SA_MA7
SB_MA_8	AE21	SA_MA8
SB_MA_9	AL20	SA_MA9
SB_MA_10	AE22	SA_MA10
SB_MA_11	AE26	SA_MA11
SB_MA_12	AE26	SA_MA12
SB_MA_13	AE20	SA_MA13

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<<>SA_DQS[0..7] (8)

<<>SA_MA[0..13] (8)

<<>SA_CAS# (8)

<<>SA_RAS# (8)

<<>SA_WE# (8)

VTT

U22H

T25	VCC_NCTF1
R25	VCC_NCTF2
P25	VCC_NCTF3
N25	VCC_NCTF4
M25	VCC_NCTF5
P24	VCC_NCTF6
N24	VCC_NCTF7
M24	VCC_NCTF8
Y22	VCC_NCTF9
W22	VCC_NCTF10
V22	VCC_NCTF11
U22	VCC_NCTF12
T22	VCC_NCTF13
R22	VCC_NCTF14
Q22	VCC_NCTF15
M22	VCC_NCTF16
Y21	VCC_NCTF17
W21	VCC_NCTF18
V21	VCC_NCTF19
U21	VCC_NCTF20
T21	VCC_NCTF21
R21	VCC_NCTF22
Q21	VCC_NCTF23
N21	VCC_NCTF24
M21	VCC_NCTF25
Y20	VCC_NCTF26
W20	VCC_NCTF27
V20	VCC_NCTF28
U20	VCC_NCTF29
T20	VCC_NCTF30
R20	VCC_NCTF31
Q20	VCC_NCTF32
N20	VCC_NCTF33
M20	VCC_NCTF34
Y19	VCC_NCTF35
W19	VCC_NCTF36
V19	VCC_NCTF37
U19	VCC_NCTF38
T19	VCC_NCTF39
R19	VCC_NCTF40
Q19	VCC_NCTF41
N19	VCC_NCTF42
M19	VCC_NCTF43
Y17	VCC_NCTF44
W17	VCC_NCTF45
V17	VCC_NCTF46
U17	VCC_NCTF47
T17	VCC_NCTF48
R17	VCC_NCTF49
Q17	VCC_NCTF50
N17	VCC_NCTF51
M17	VCC_NCTF52
Y15	VCC_NCTF53
W15	VCC_NCTF54
V15	VCC_NCTF55
U15	VCC_NCTF56
T15	VCC_NCTF57
R15	VCC_NCTF58
Q15	VCC_NCTF59
N15	VCC_NCTF60
M15	VCC_NCTF61
Y14	VCC_NCTF62
W14	VCC_NCTF63
V14	VCC_NCTF64
U14	VCC_NCTF65
T14	VCC_NCTF66
R14	VCC_NCTF67
Q14	VCC_NCTF68
N14	VCC_NCTF69
M14	VCC_NCTF70

NCTF

VCCAUX_NCTF1	AD25
VCCAUX_NCTF2	AG25
VCCAUX_NCTF3	AB25
VCCAUX_NCTF4	AD24
VCCAUX_NCTF5	AC24
VCCAUX_NCTF6	AD22
VCCAUX_NCTF7	AD21
VCCAUX_NCTF8	AD20
VCCAUX_NCTF9	AD19
VCCAUX_NCTF10	AD18
VCCAUX_NCTF11	AD17
VCCAUX_NCTF12	AD16
VCCAUX_NCTF13	AD15
VCCAUX_NCTF14	AD14
VCCAUX_NCTF15	AD13
VCCAUX_NCTF16	Y13
VCCAUX_NCTF17	W13
VCCAUX_NCTF18	V13
VCCAUX_NCTF19	U13
VCCAUX_NCTF20	T13
VCCAUX_NCTF21	R13
VCCAUX_NCTF22	Q13
VCCAUX_NCTF23	N13
VCCAUX_NCTF24	M13
VCCAUX_NCTF25	AD12
VCCAUX_NCTF26	Y12
VCCAUX_NCTF27	W12
VCCAUX_NCTF28	V12
VCCAUX_NCTF29	U12
VCCAUX_NCTF30	T12
VCCAUX_NCTF31	R12
VCCAUX_NCTF32	P12
VCCAUX_NCTF33	N12
VCCAUX_NCTF34	M12
VCCAUX_NCTF35	AD11
VCCAUX_NCTF36	AD10
VCCAUX_NCTF37	K10
VCCAUX_NCTF38	AN33
VSS_NCTF1	AA25
VSS_NCTF2	V25
VSS_NCTF3	U25
VSS_NCTF4	AA22
VSS_NCTF5	AA21
VSS_NCTF6	AA20
VSS_NCTF7	AA19
VSS_NCTF8	AA18
VSS_NCTF9	AA17
VSS_NCTF10	AA16
VSS_NCTF11	AA15
VSS_NCTF12	AA14
VSS_NCTF13	AA13
VSS_NCTF14	A4
VSS_NCTF15	A33
VSS_NCTF16	B2
VSS_NCTF17	AN1
VSS_NCTF18	C1
VSS_NCTF19	

CFG_19

CFG_19: DMI Lane Reversal
0= default (internal pull-down)
1= Reversal Lanes
(945GSE does not support)

RESERVED10	K25
RESERVED11	R24
RESERVED12	T24
RESERVED13	K21
RESERVED14	K19
RESERVED15	K20
RESERVED16	K24
RESERVED17	K22
RESERVED18	J17
RESERVED19	K23
RESERVED20	K17
RESERVED21	K12
RESERVED22	K13
RESERVED23	K16
RESERVED24	K15
RESERVED25	

945GSE

+1.5VRUN

VTT

U22E
945GSE

VSS

U16	VSS_110
AH16	VSS_108
B17	VSS_107
F17	VSS_106
M17	VSS_105
K17	VSS_104
D18	VSS_103
AH18	VSS_102
U18	VSS_101
AE18	VSS_99
AH18	VSS_98
AE18	VSS_97
W19	VSS_96
D20	VSS_95
AE20	VSS_94
AK20	VSS_93
AM20	VSS_92
F21	VSS_91
J21	VSS_89
E22	VSS_88
G22	VSS_86
AJ22	VSS_85
AM22	VSS_84
B23	VSS_82
F23	VSS_81
AE23	VSS_80
AK23	VSS_79
AG23	VSS_78
G25	VSS_77
J25	VSS_76
AE25	VSS_75
AK25	VSS_74
AG25	VSS_73
AE25	VSS_72
AK25	VSS_71
AG25	VSS_70
AE25	VSS_69
AK25	VSS_68
AG25	VSS_67
AE25	VSS_66
AK25	VSS_65
AG25	VSS_64
AE25	VSS_63
AK25	VSS_62
AG25	VSS_61
AE25	VSS_60
AK25	VSS_59
AG25	VSS_58
AE25	VSS_57
AK25	VSS_56
AG25	VSS_55
AE25	VSS_54
AK25	VSS_53
AG25	VSS_52
AE25	VSS_51
AK25	VSS_50
AG25	VSS_49
AE25	VSS_48
AK25	VSS_47
AG25	VSS_46
AE25	VSS_45
AK25	VSS_44
AG25	VSS_43
AE25	VSS_42
AK25	VSS_41
AG25	VSS_40
AE25	VSS_39
AK25	VSS_38
AG25	VSS_37
AE25	VSS_36
AK25	VSS_35
AG25	VSS_34
AE25	VSS_33
AK25	VSS_32
AG25	VSS_31
AE25	VSS_30
AK25	VSS_29
AG25	VSS_28
AE25	VSS_27
AK25	VSS_26
AG25	VSS_25
AE25	VSS_24
AK25	VSS_23
AG25	VSS_22
AE25	VSS_21
AK25	VSS_20
AG25	VSS_19
AE25	VSS_18
AK25	VSS_17
AG25	VSS_16
AE25	VSS_15
AK25	VSS_14
AG25	VSS_13
AE25	VSS_12
AK25	VSS_11
AG25	VSS_10
AE25	VSS_9
AK25	VSS_8
AG25	VSS_7
AE25	VSS_6
AK25	VSS_5
AG25	VSS_4
AE25	VSS_3
AK25	VSS_2
AG25	VSS_1
AE25	VSS_0



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MS-N033

Size Custom	Document Description 945GSE_DDR	Rev 0A
Date: Thursday, November 13, 2008	Sheet 6 of 37	

945 GMS Power

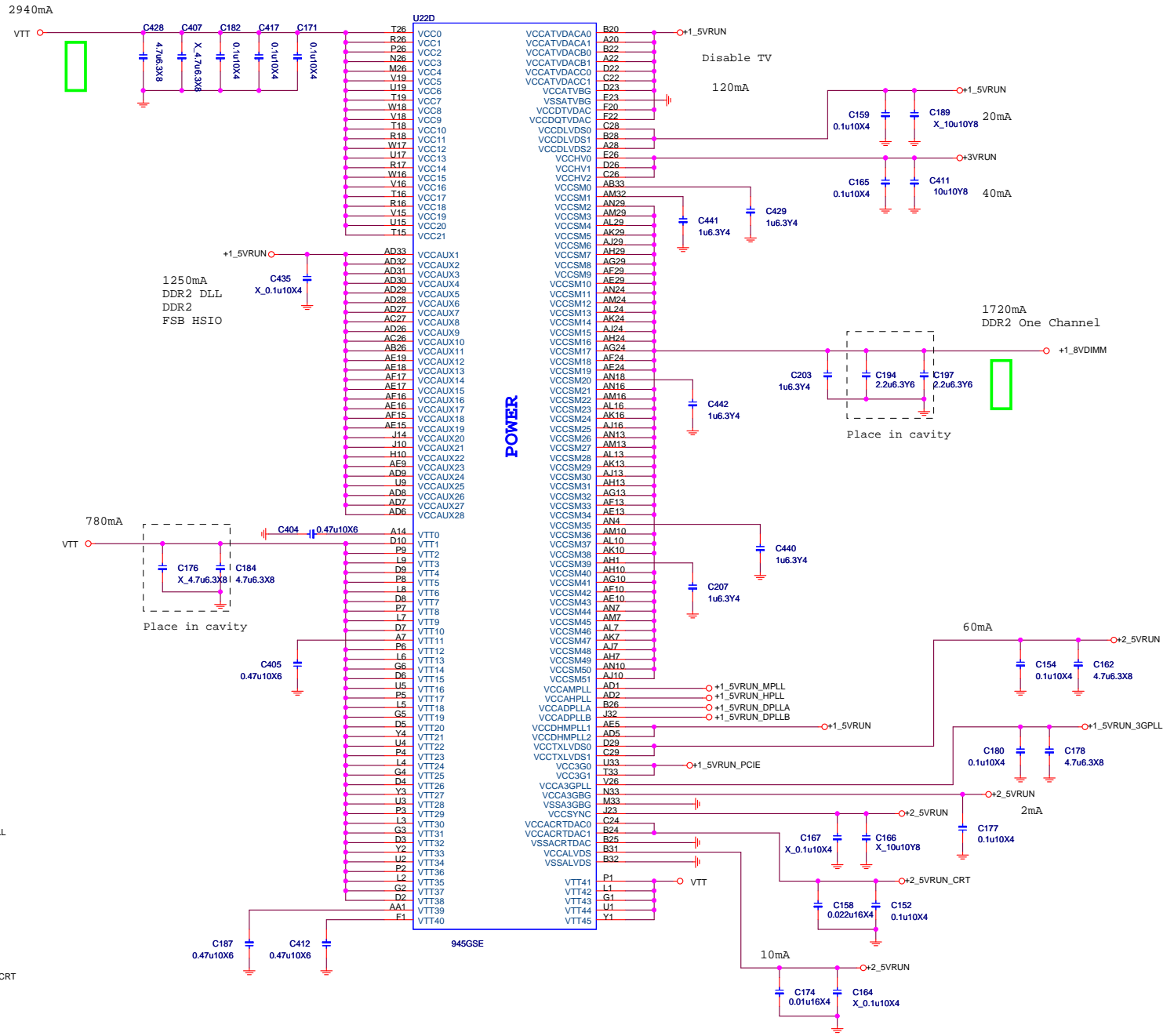
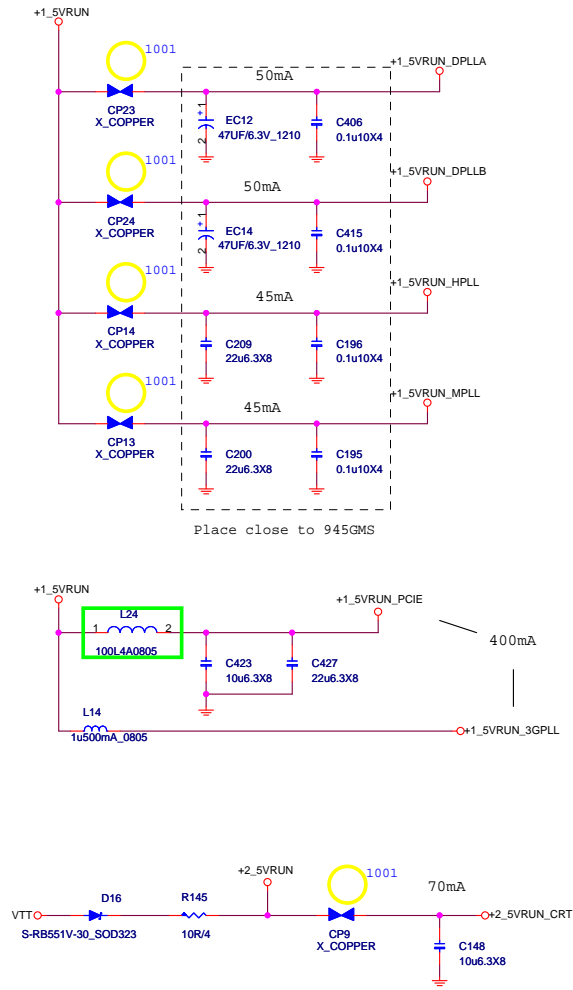
VTT=> 3.72A

+1_5VRUN=> 1.98A

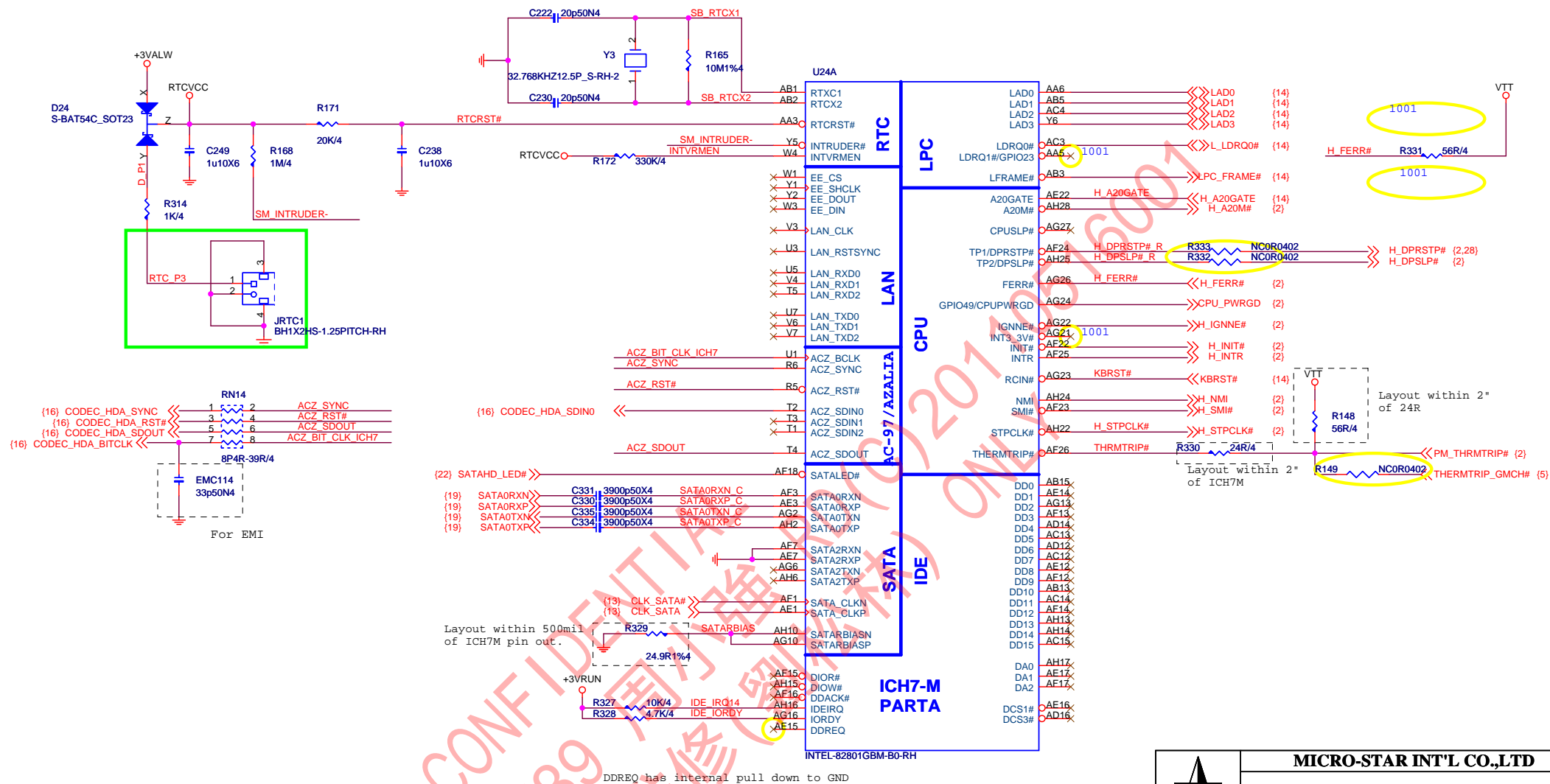
+1_8VDIMM=> 1.72A

+2_5VRUN=>142mA

+3VRUN=> 40mA



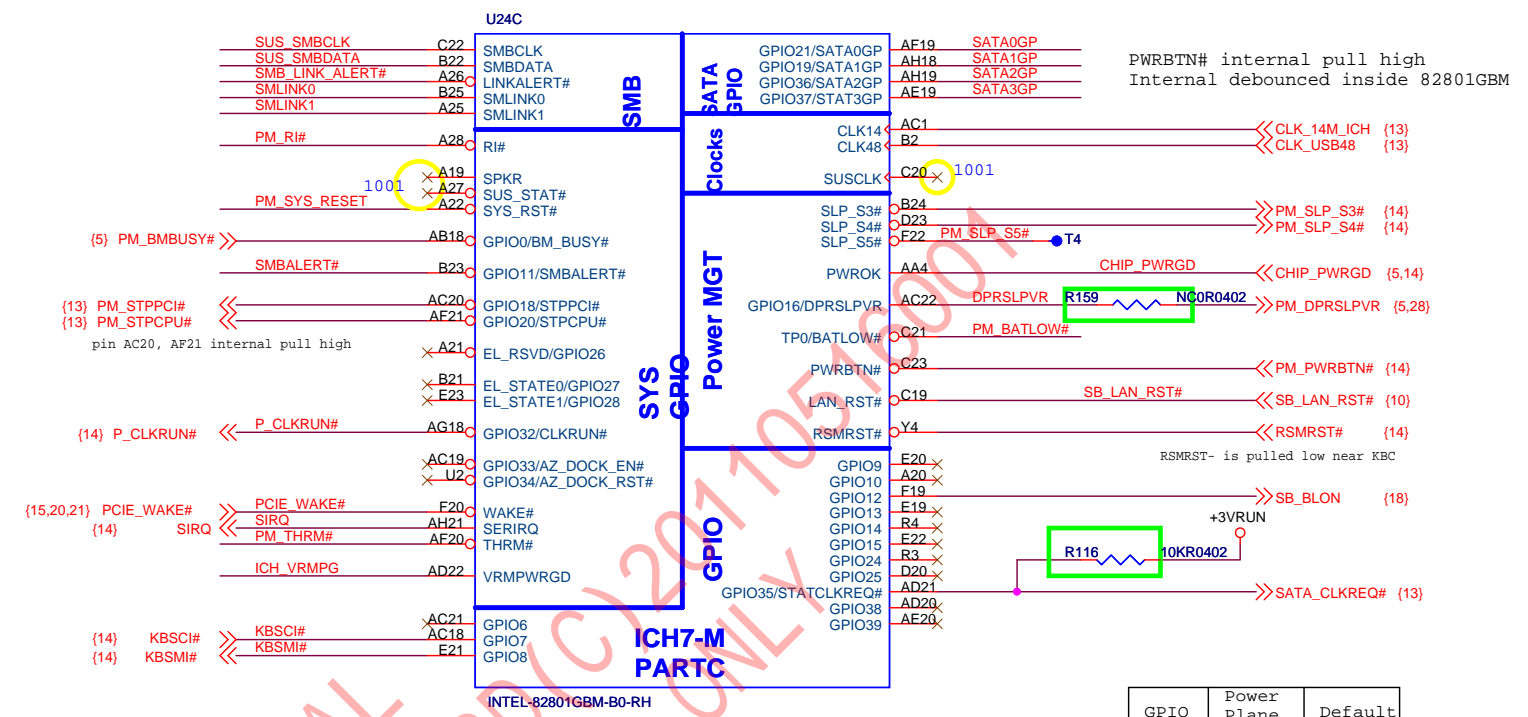
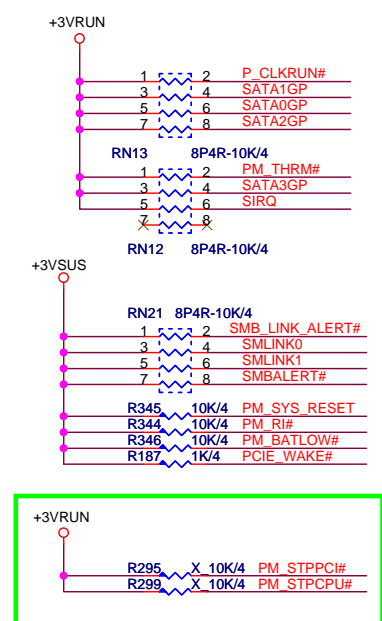




MICRO-STAR INT'L CO.,LTD

MS-N033

Size Custom	Document Description ICH7M_CPU, LPC, SATA, HDA	Rev 0A
Date: Thursday, November 13, 2008		Sheet 9 of 37



GPIO	Power Plane	Default
6,7	Core	GPI
8~10	Resume	GPI
12~15	Resume	GPI
24,25	Resume	GPO
38,39	Core	GPI

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MS-N033

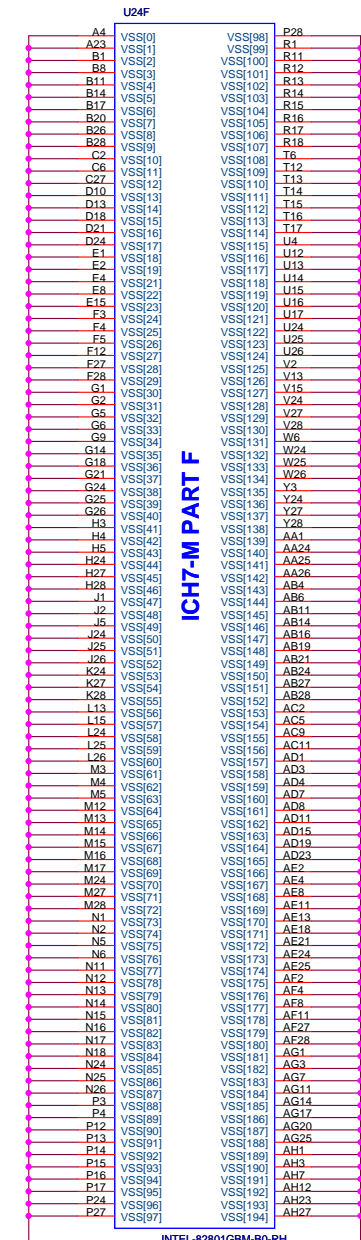
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Rev 0A

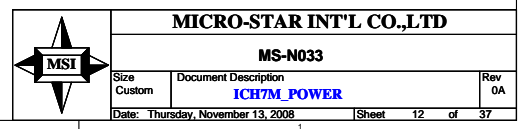
ICH7M_GPIO, CLK, SM

Date: Thursday, November 13, 2008
Sheet 11 of 37

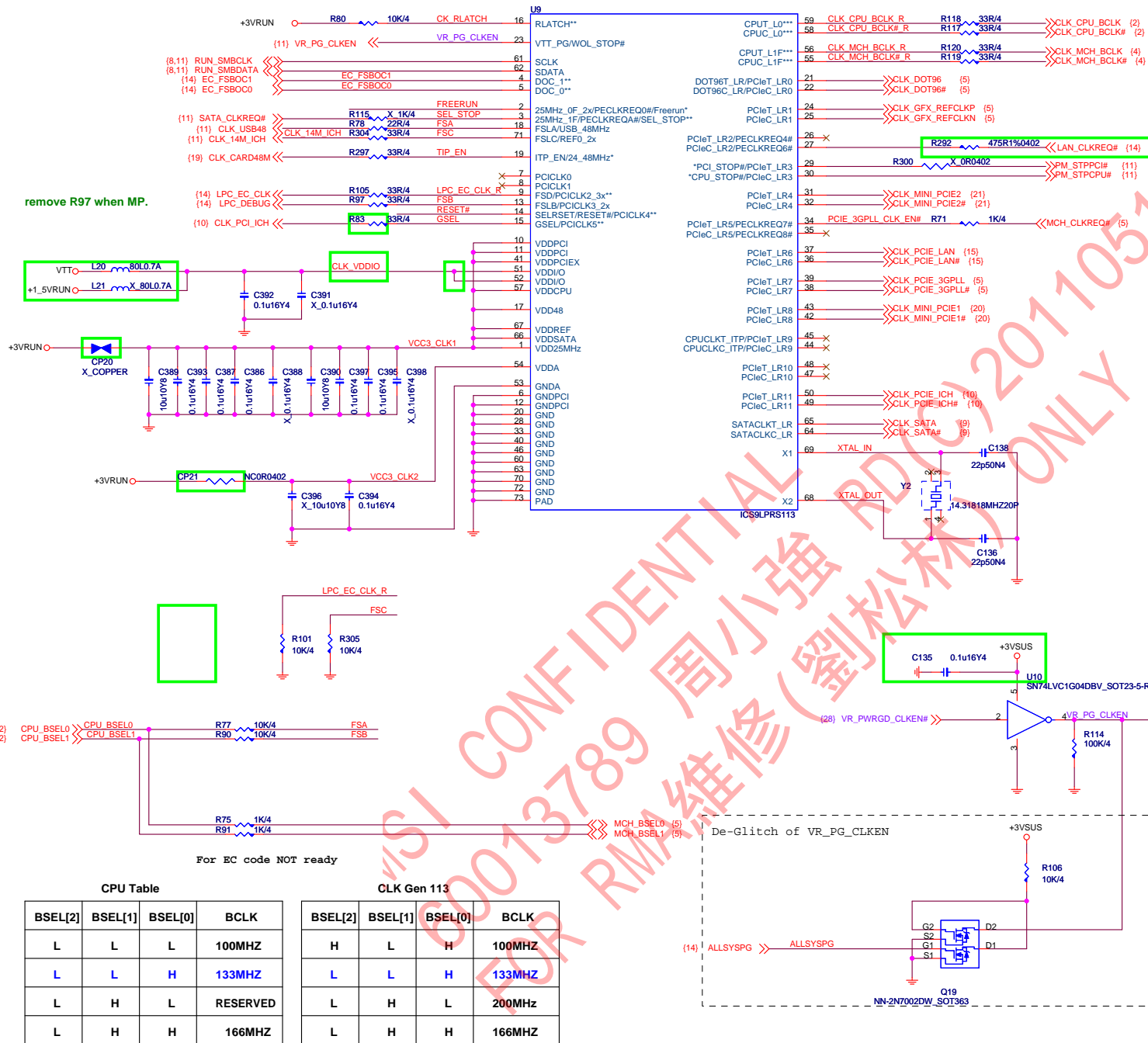
[illegible]

ICH7-M PART F

PIN AA2,Y7,K7,C28,G20 : VccSus 1.05V for RTCVCC



CLOCK GEN STRAPING



1 => Pin21/22 96MHz
0 => Pin21/22 100MHz



L:PCICLK4
H:RESET*
to be WDT rest=> HI



LPRS113	LPRS110
TIP_EN=0 => PCIE_X9,	TIP_EN=0 => 48MHz,
TIP_EN=1 => CPU_ITP	TIP_EN=1 => 24MHz

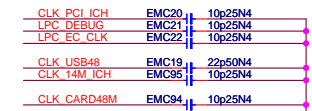




```
Selects pin 29/30
1 = PCI_STOP#/CPU_STOP#
0 =PCIEX CLK output
```



EMI



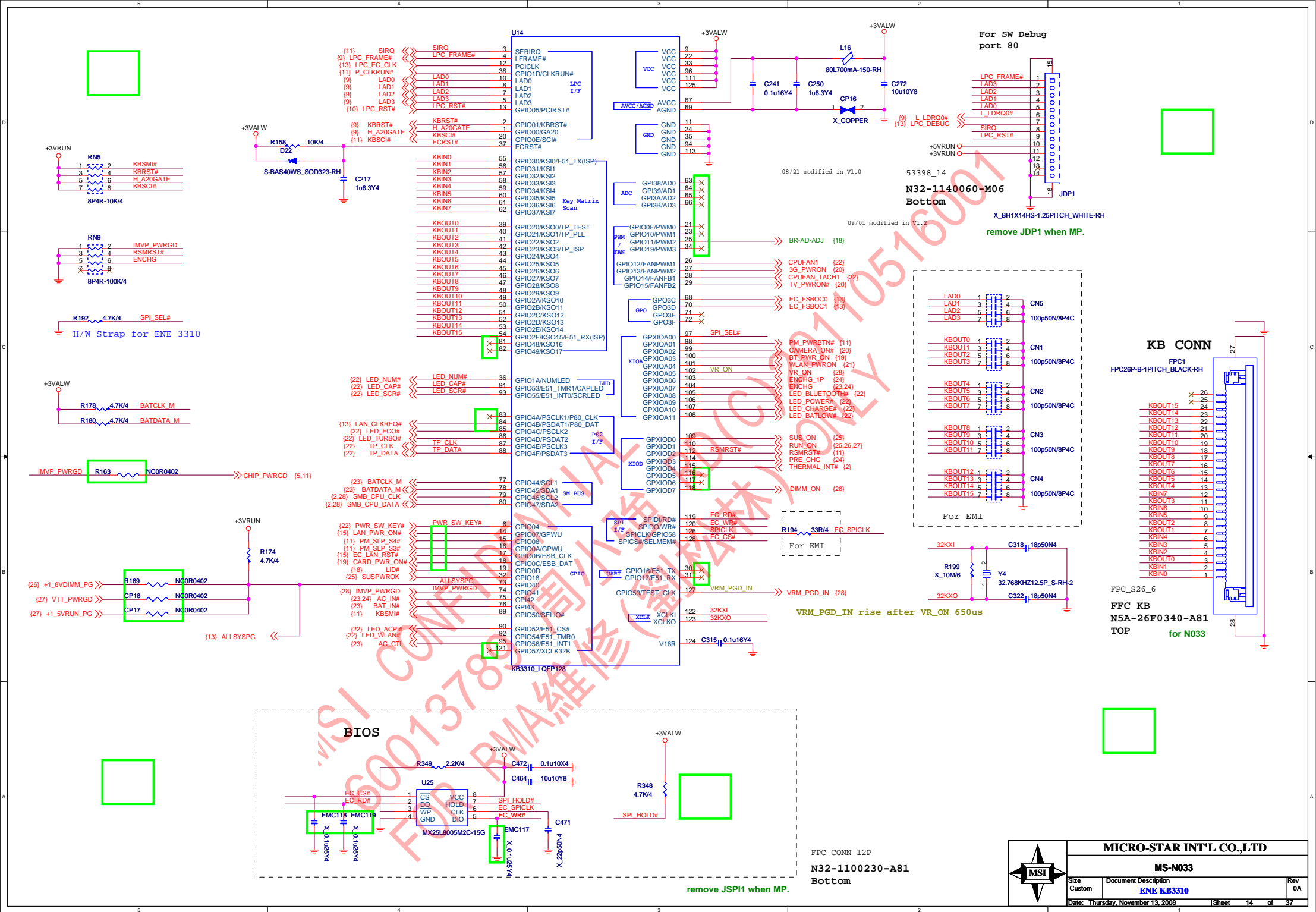
08/21 modified in V1.0



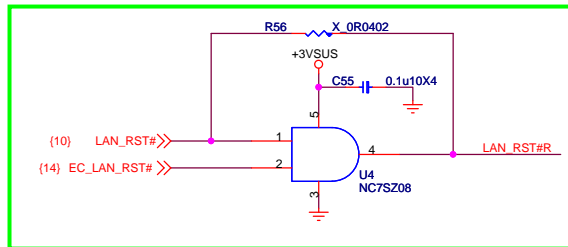
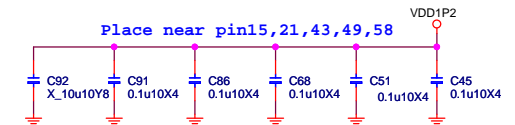
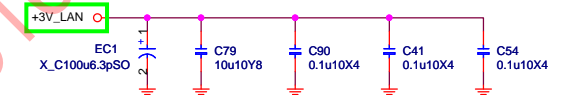
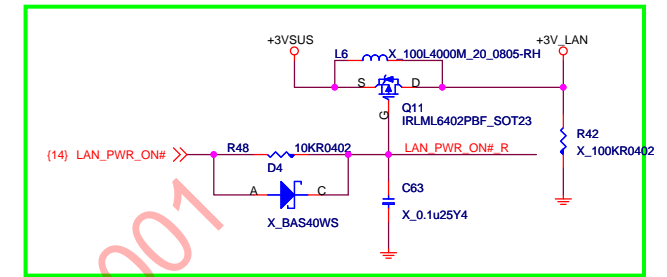
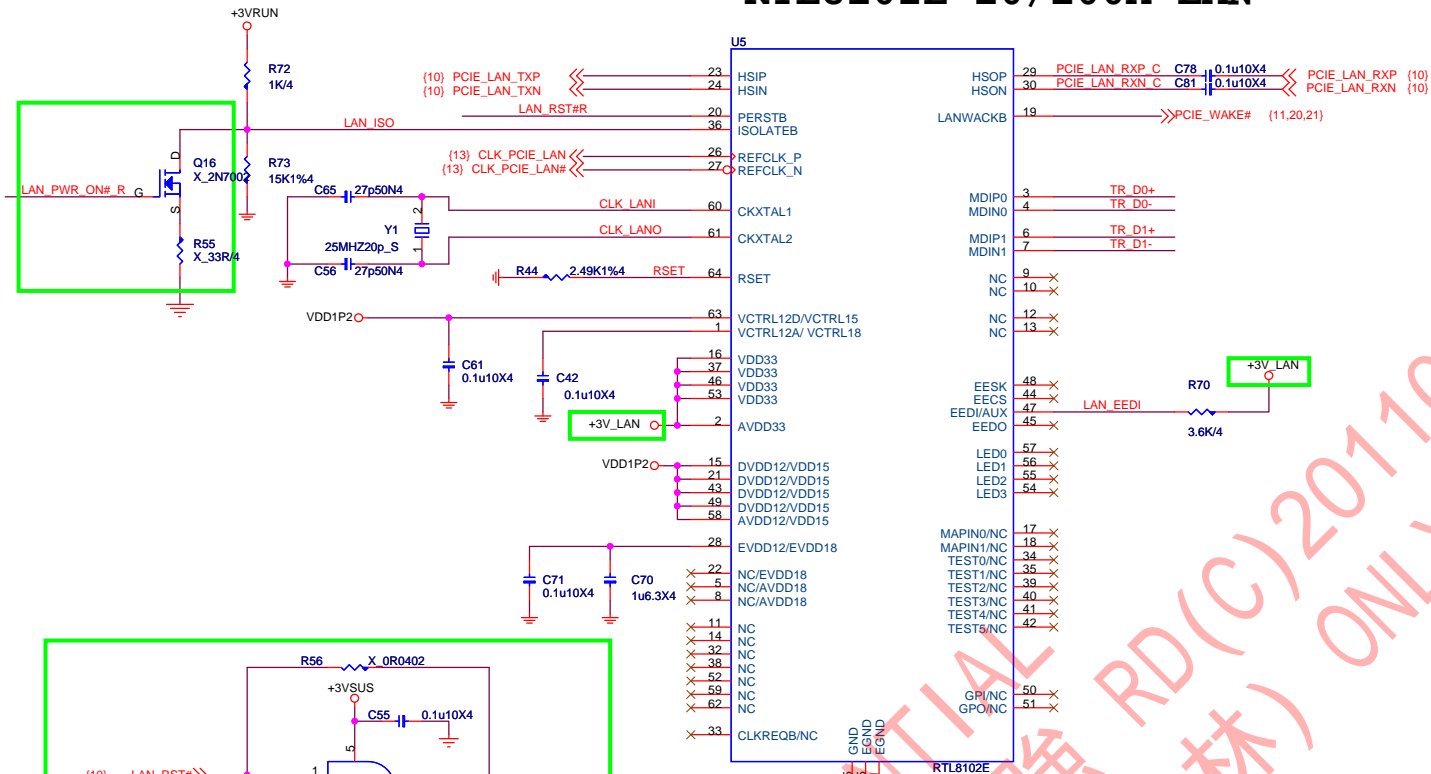
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MS-N033

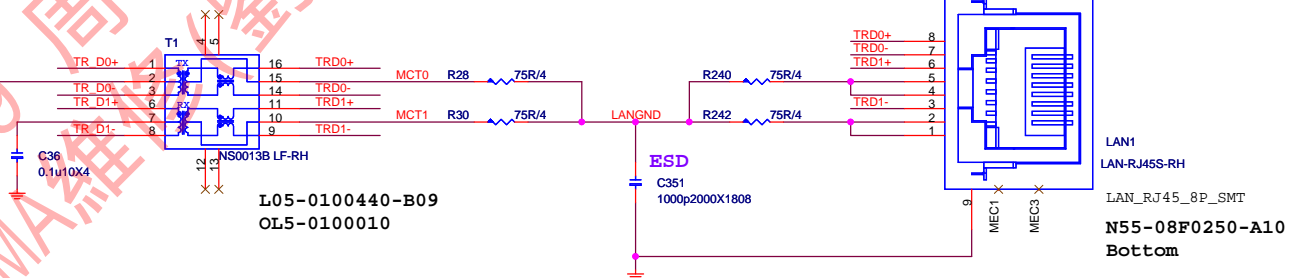
Size Custom	Document Description CLK GEN_113	Rev 0A
Date: Thursday, November 13, 2008	Sheet 13 of 37	



RTL8102E 10/100M LAN



LAN MAGNETICS



POWER			
BOOT DEVICE	VDD1P2	VDD1P8	VDD33
8102E	1.2V	NC	3.3V

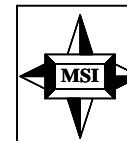
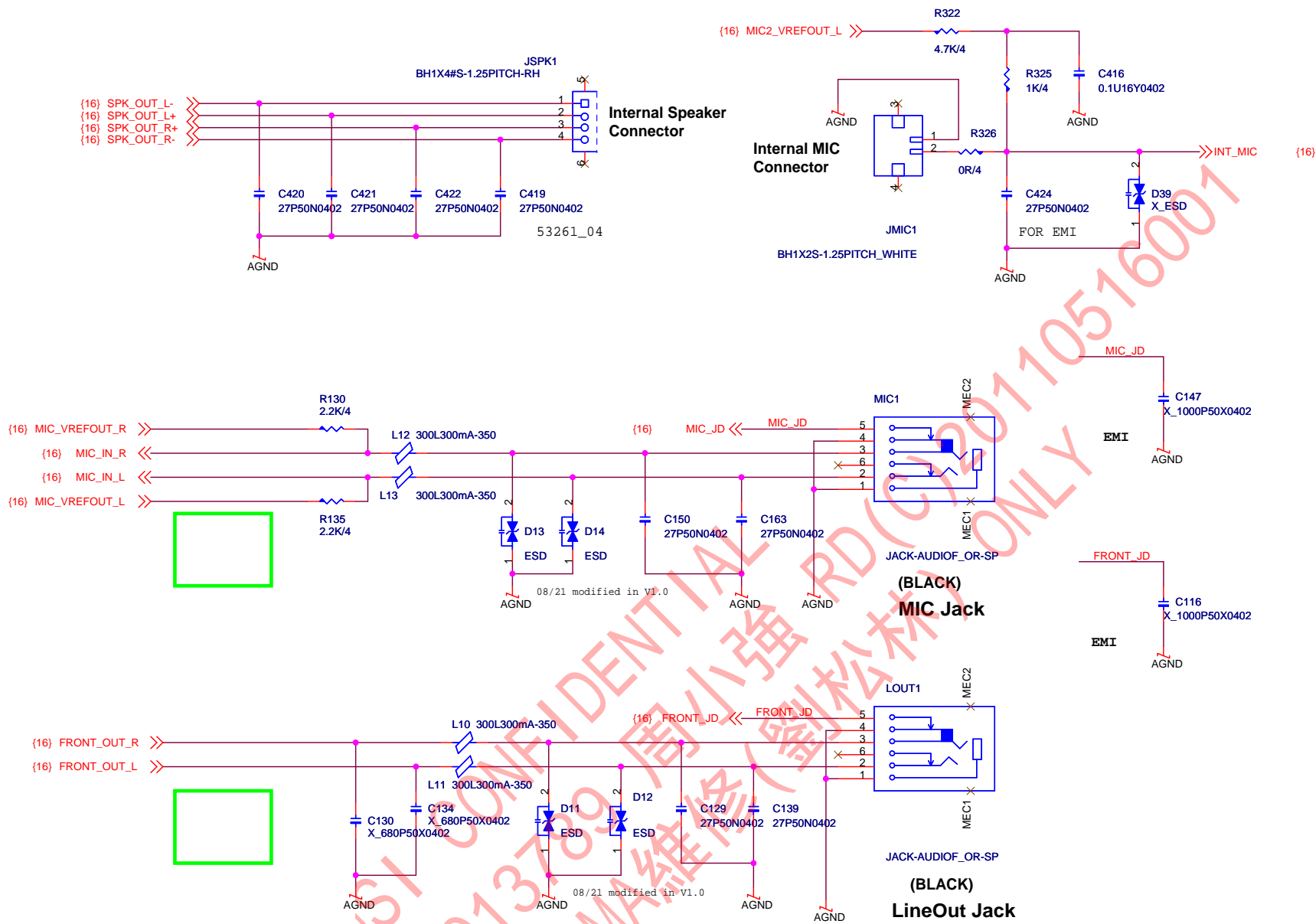
365mA



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MS-N033

Size Custom	Document Description LAN_RTL8102E	Rev 0A
Date: Thursday, November 13, 2008		Sheet 15 of 37

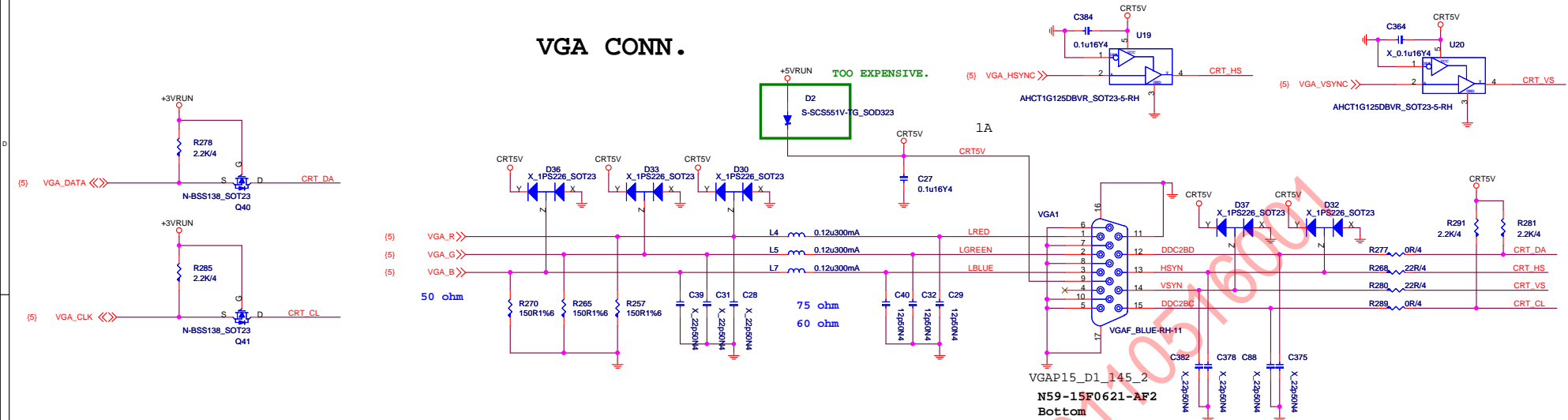


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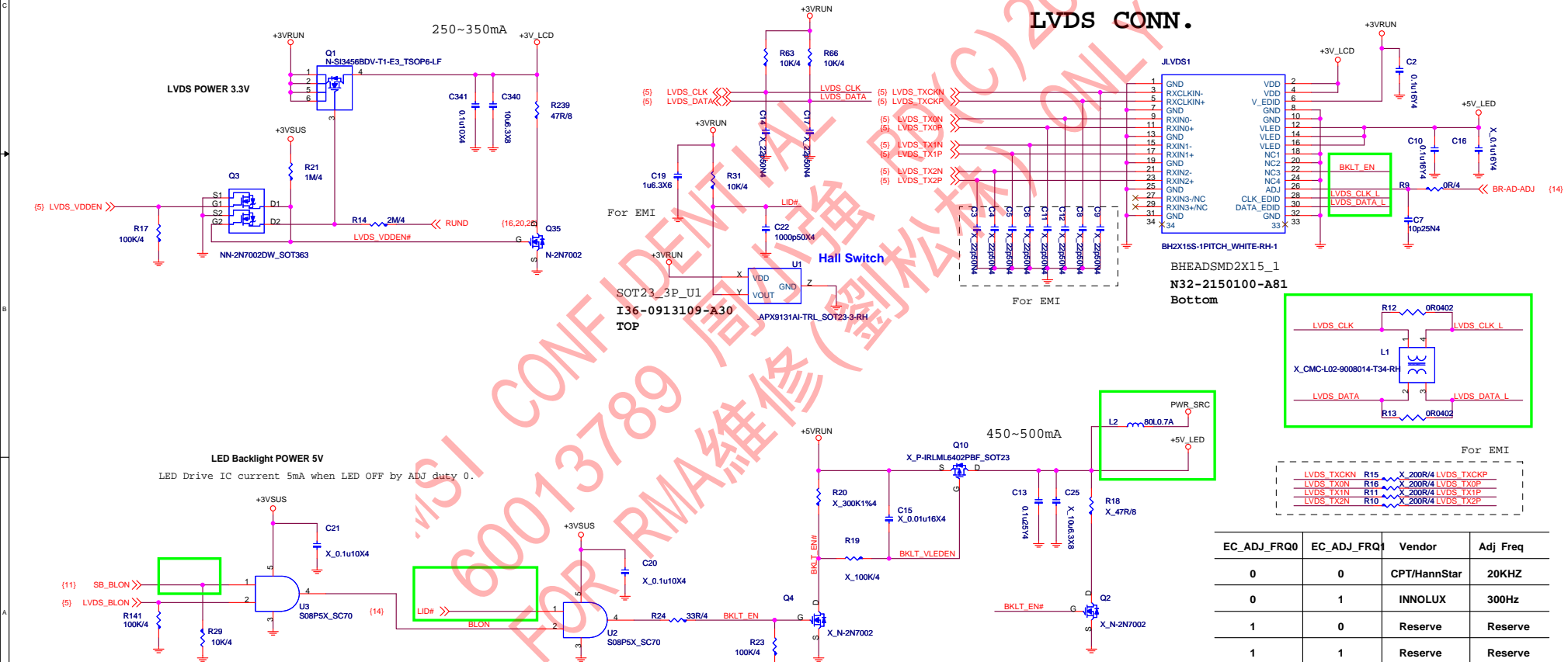
MS-N033

Size Custom	Document Description Audio JACKS	Rev 0A
Date: Thursday, November 13, 2008	Sheet 17 of 37	

VGA CONN.

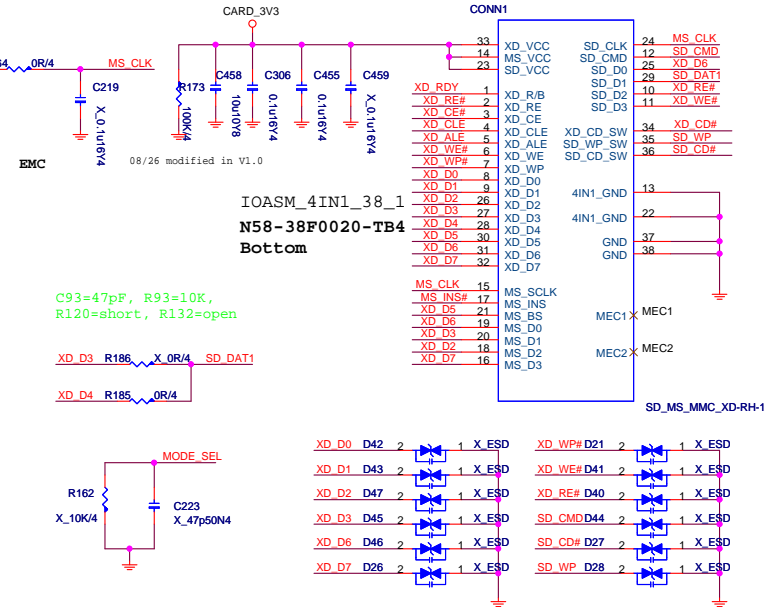


LVDS CONN.



EC_ADJ_FRQ0	EC_ADJ_FRQ	Vendor	Adj Freq
0	0	CPT/HannStar	20KHZ
0	1	INNOLUX	300Hz
1	0	Reserve	Reserve
1	1	Reserve	Reserve

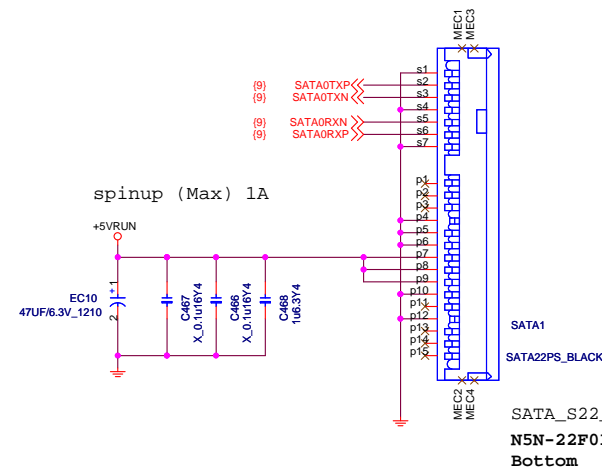
Flash Card Socket



08/21 modified in V1.0 for EMI

SATA,2.5 inch,80GB,5400RPM	
WD	S71-2408505-W36
Fujitsu	S71-2408511-F06
Toshiba	S71-2408517-T14

SATA HDD CONN



Media I/F(Chip)	SD Card	Memory Stick	xD Card
XD_RDY	X	X	XD_R/B
XD_RE#/SD_DAT2	SD_D2	X	XD_RE
XD_CE#	X	X	XD_CE
XD_CLE	X	X	XD_CLE
XD_ALE	X	X	XD_ALE
XD_WE#/SD_DAT3	SD_D3	X	XD_WE
XD_WP#/SD_DAT4/MS_D7	X	X	XD_WP
XD_D0/SD_DAT0/MS_D6	X	X	XD_D0
XD_D1/SD_CLK/MS_CLK	SD_CLK	MS_CLK	XD_D1
XD_D2/SD_DAT7/MS_D2	X	MS_D2	XD_D2
XD_D3/SD_DAT1/MS_D1	SD_D1	MS_D1	XD_D3
XD_D4	X	X	XD_D4
XD_D5/MS_BS	X	MS_BS	XD_D5
XD_D6/SD_DAT0/MS_D0	SD_D0	MS_D0	XD_D6
XD_D7/SD_DAT6/MS_D3	X	MS_D3	XD_D7
XD_CD#	X	X	XD_CD_SW
SD_CMD	SD_CMD	X	X
SD_CD#	SD_CD_SW	X	X
SD_WP	SD_WP_SW	X	X
MS_INS#	X	MS_INS	X
MS_D4	X	X	X
MS_D5	X	X	X

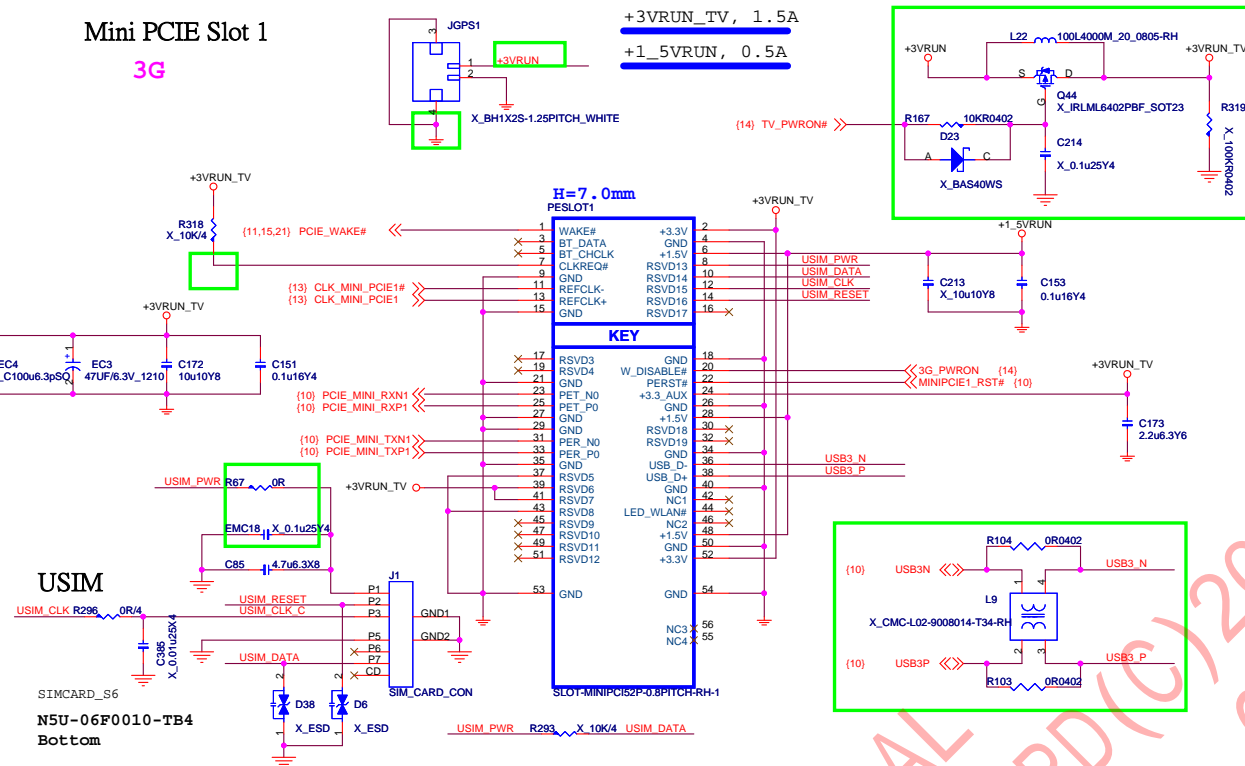


MS-N033

Size Custom	Document Description CardReader RTS5158E/ BT/ SATA HDD	Rev 0A
Date: Thursday, November 13, 2008	Sheet 19 of 37	

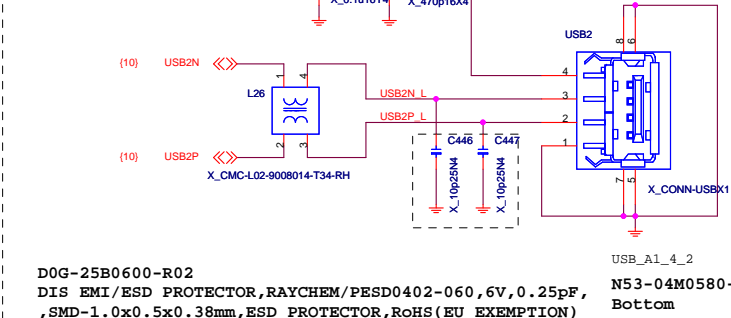
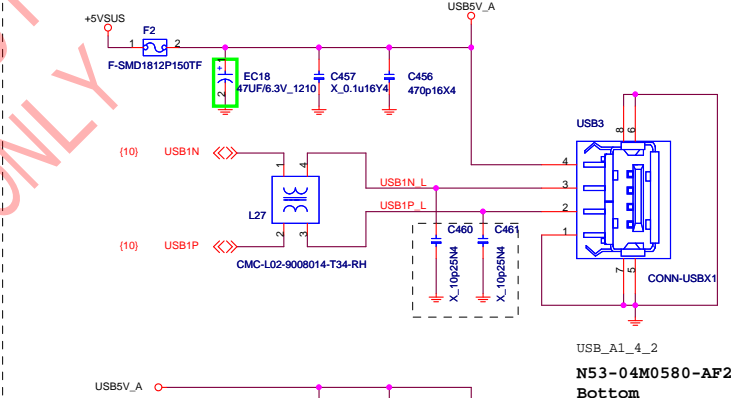
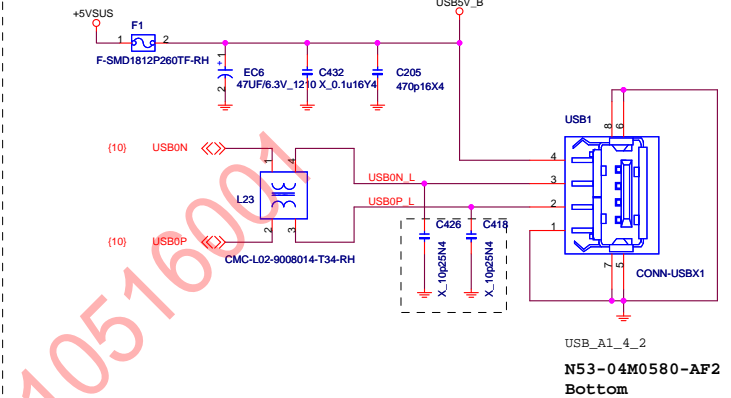
Mini PCIE Slot 1

3G



USB CONN

9/1 change 1.5A fuse to 2.6A for external USB ODD use.



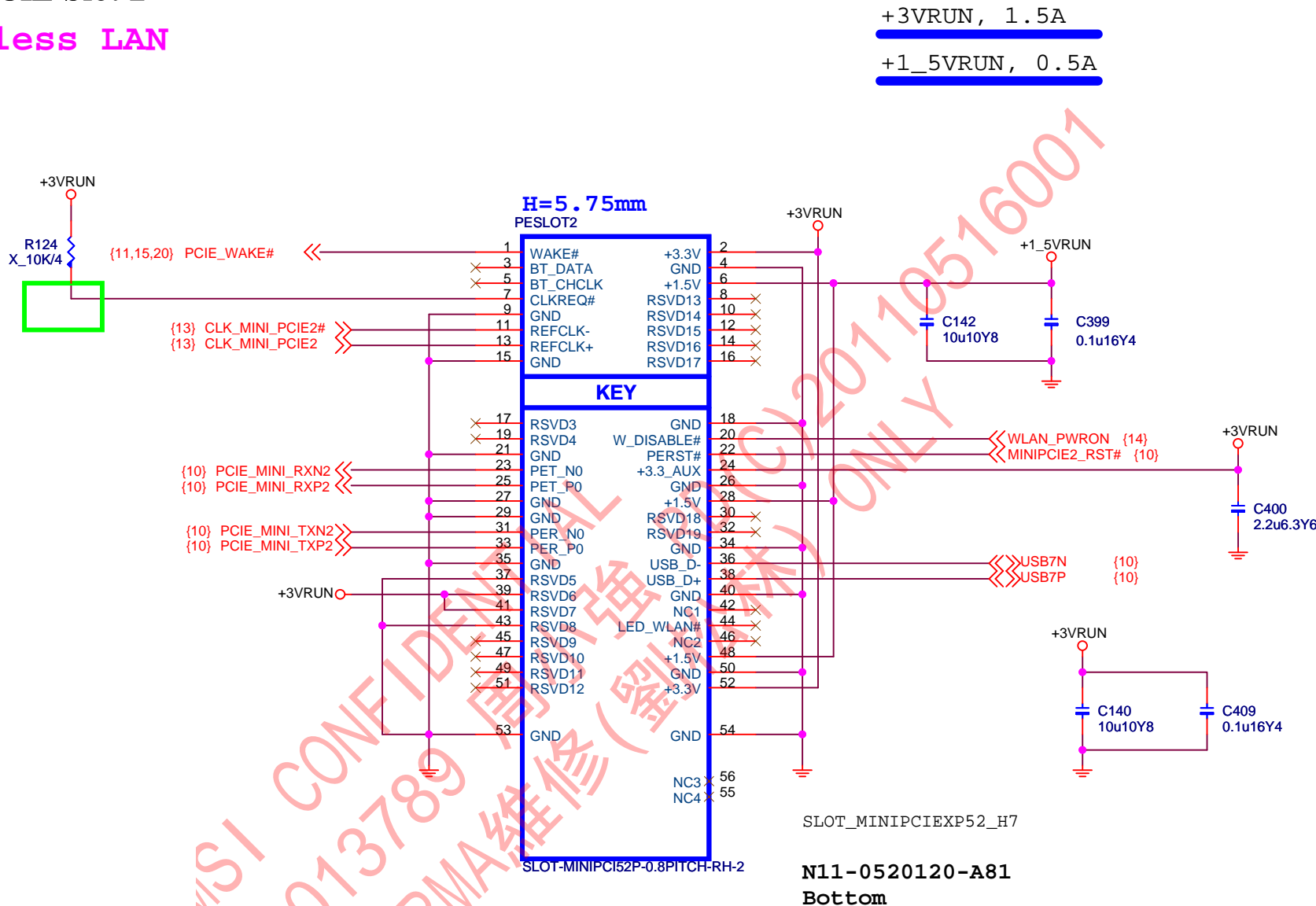
D0G-25B0600-R02
DIS EMI/ESD PROTECTOR, RAYCHEM/PESD0402-060, 6V, 0.25pF, SMD-1.0x0.5x0.38mm, ESD PROTECTOR, RoHS (EU EXEMPTION)

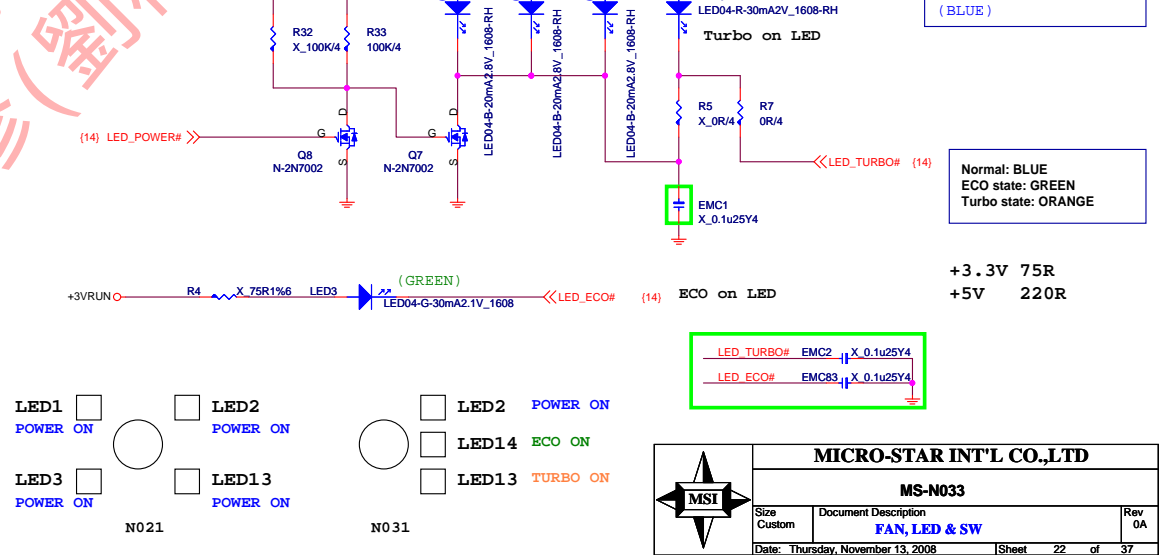
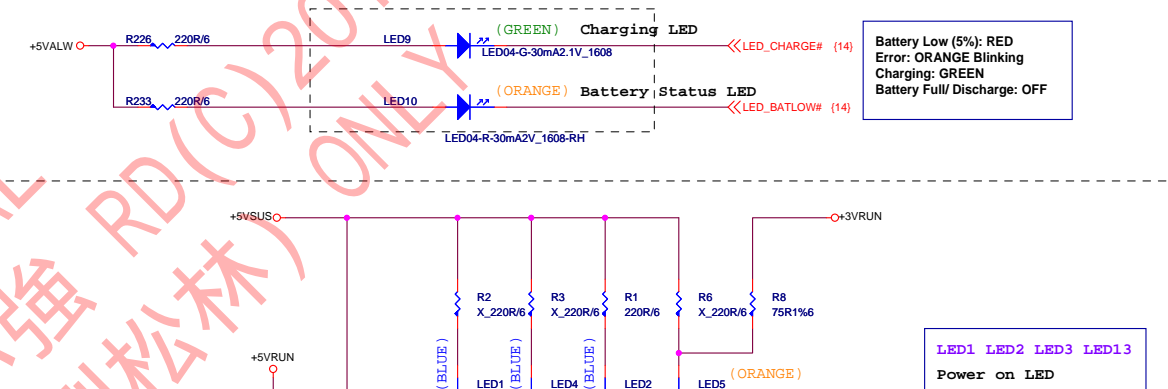
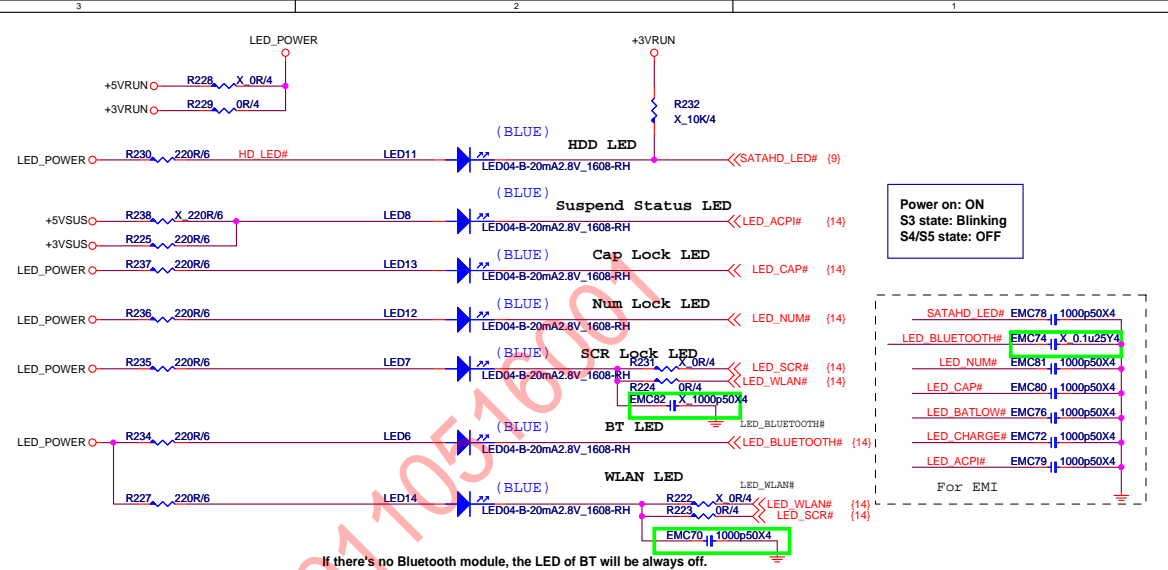
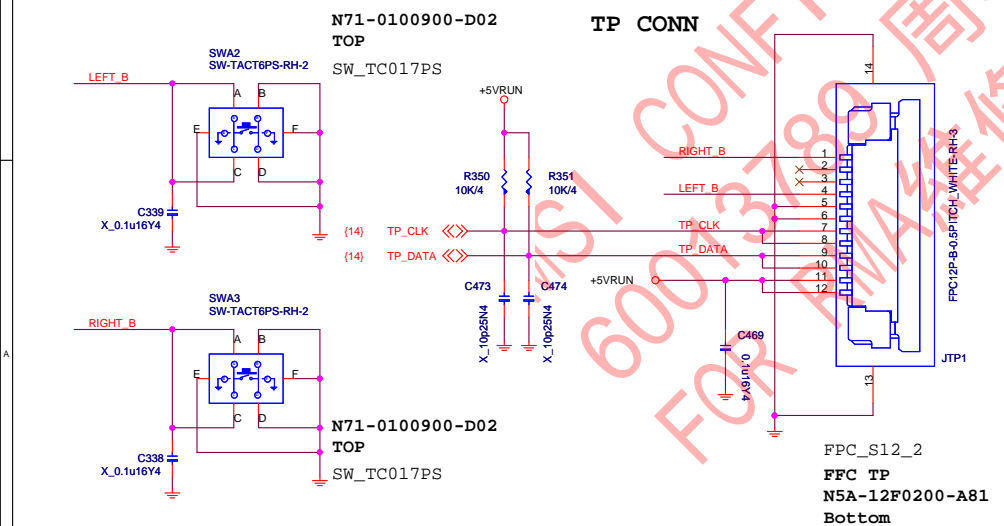
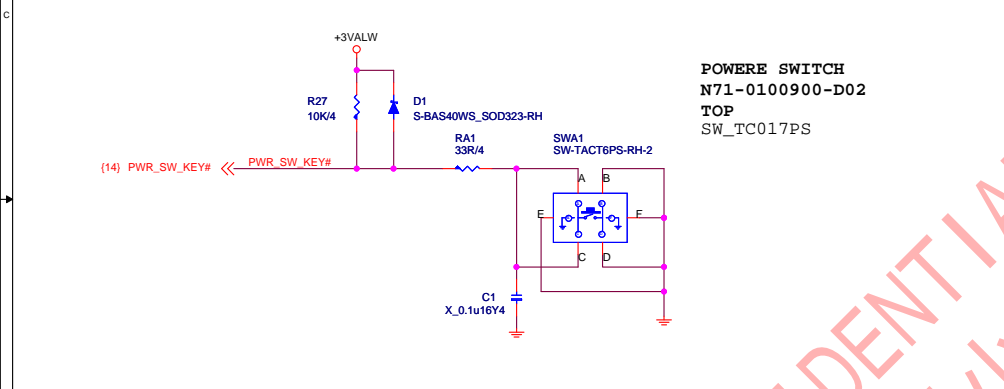
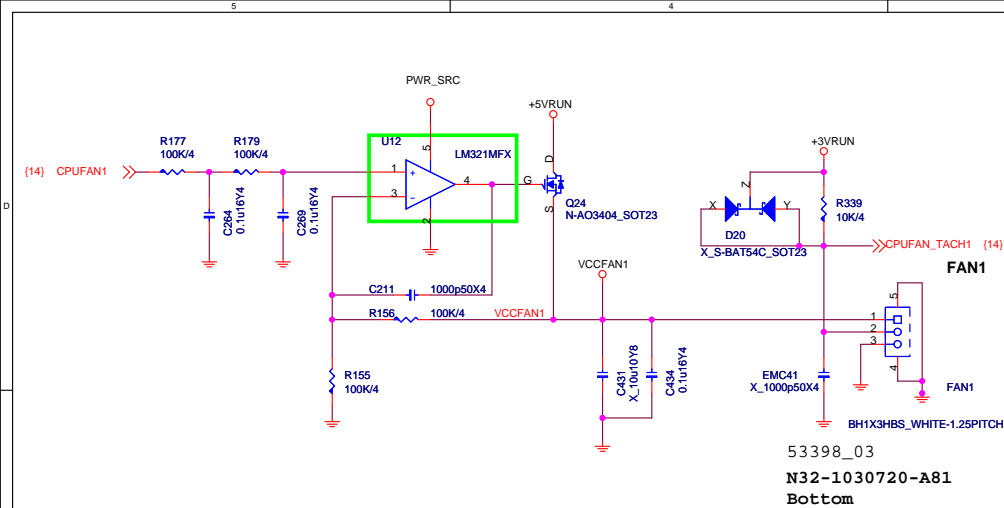


MICRO-STAR INT'L CO.,LTD			
MS-N033			
Size	Document Description	Rev	
Custom	Mini PCIE, CAMERA, USB CONN	0A	
Date: Thursday, November 13, 2008		Sheet	20 of 37

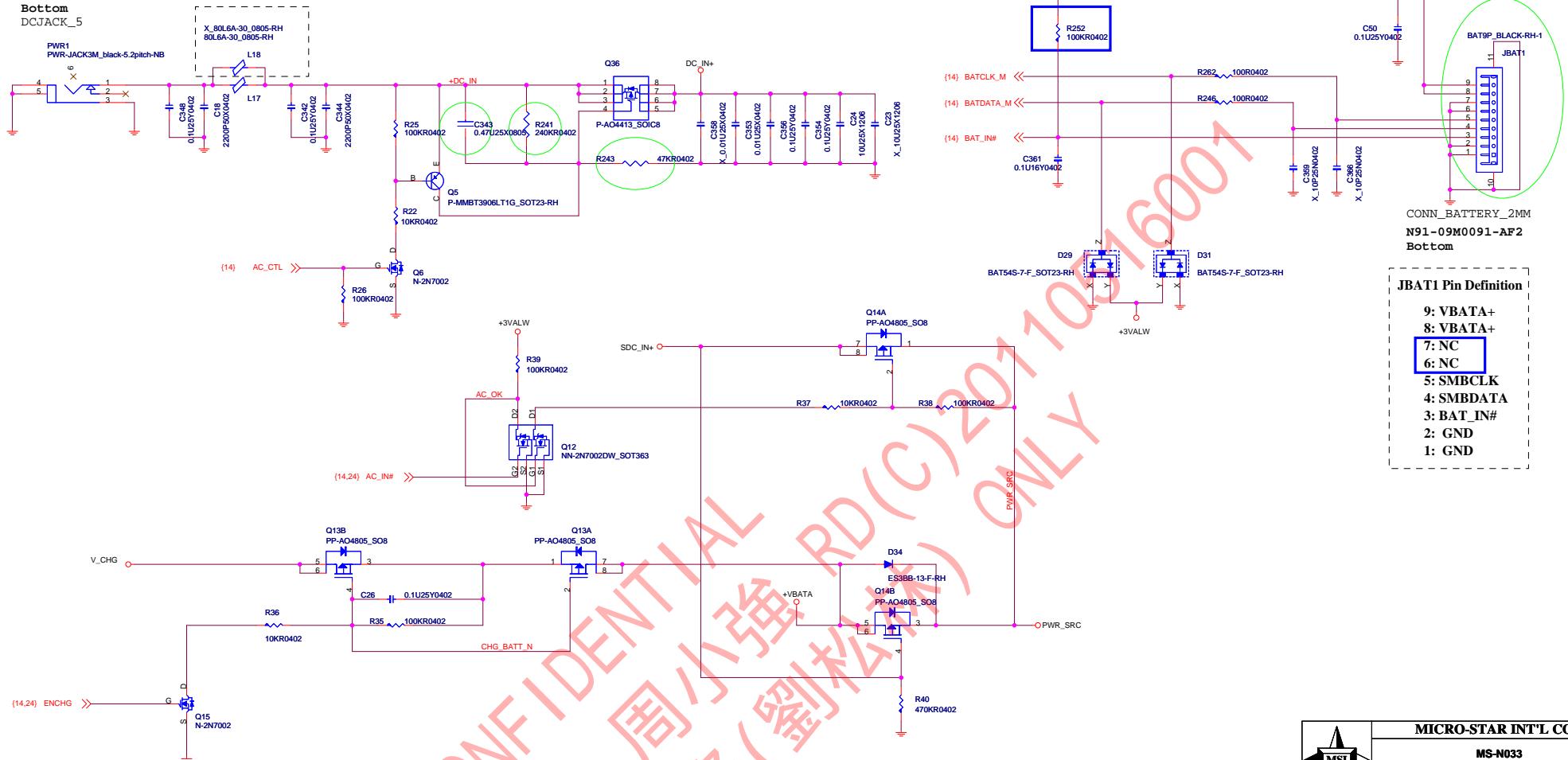
Mini PCIE Slot 2

Wireless LAN

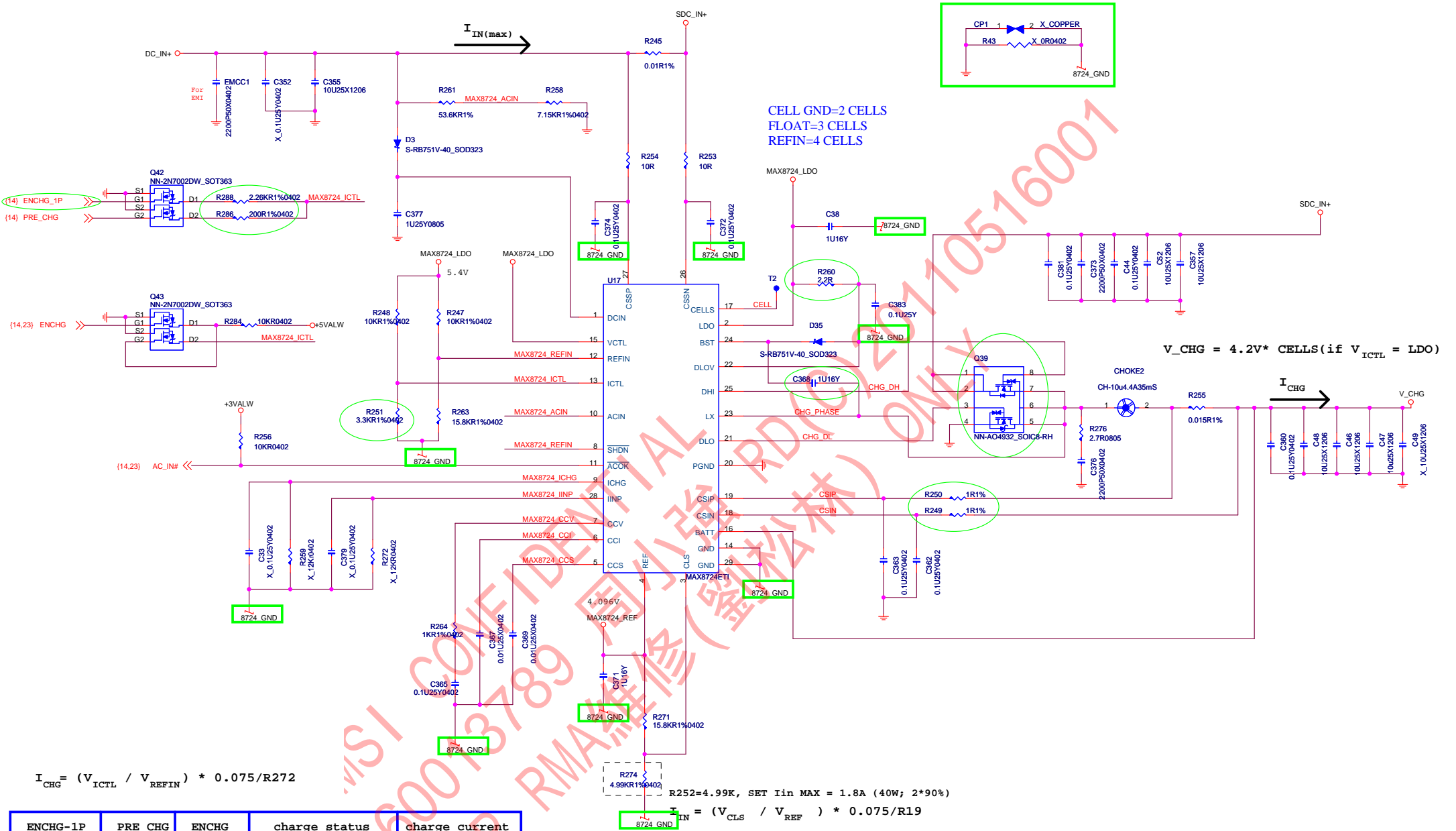




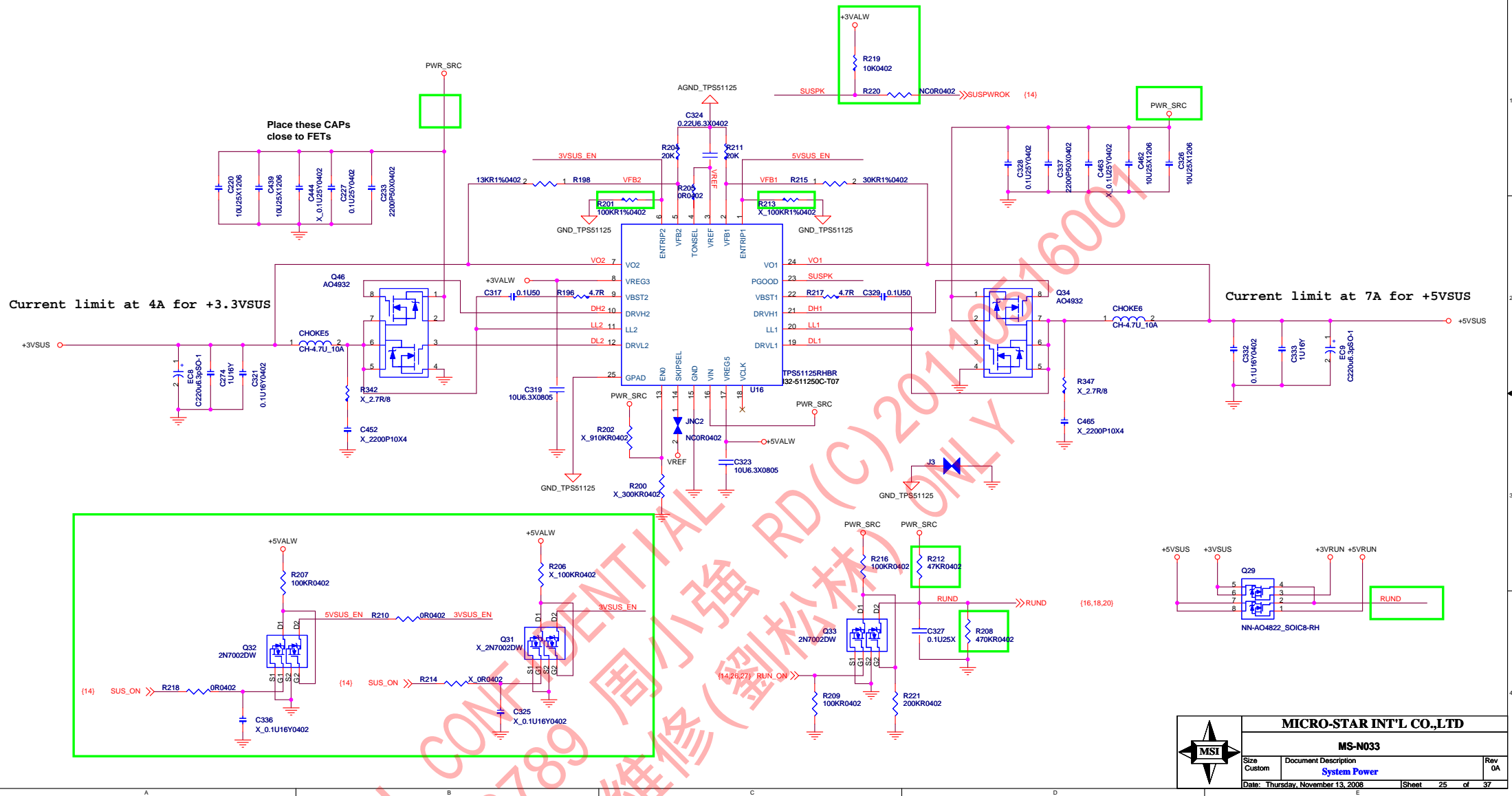
N92-03M0131-A10
N92-03M0131-H06
Bottom
DCJACK_5



Adapter= 40 W
Adapter input voltage set 20 Voltage 2 Amps



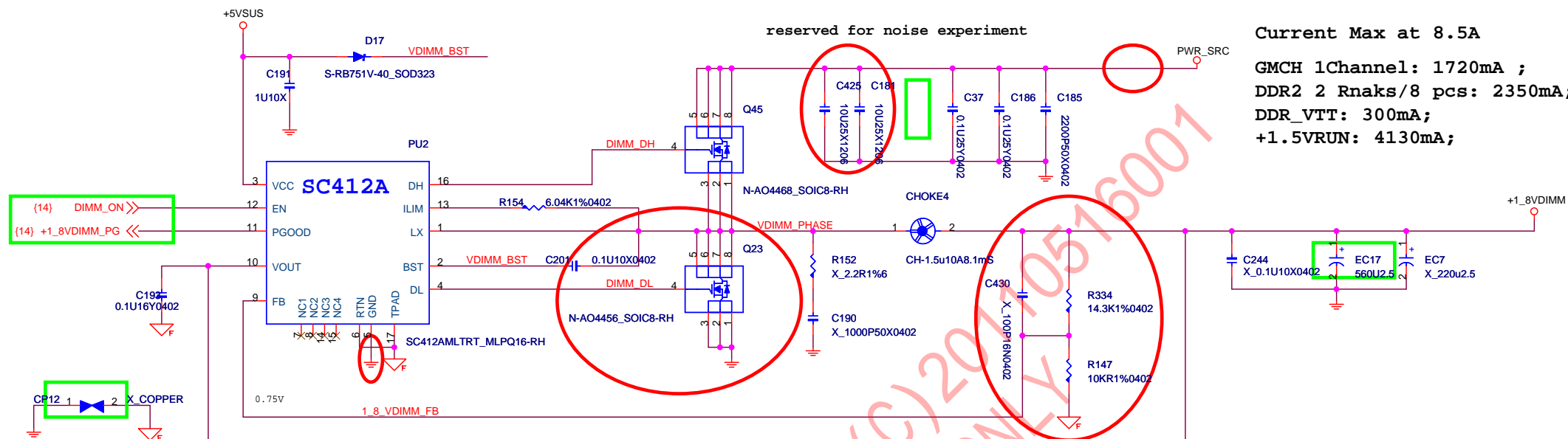
ENCHG_1P	PRE_CHG	ENCHG	charge status	charge current
0	1	1	Pre-charge	200 mA
1	0	1	3S1P-Fast charge	1.0 A
0	0	1	3S2P-Fast charge	2.05A
X	X	0	STOP CHARGE	0



+1_8VDIMM

Current Max at 8.5A

GMCH 1Channel: 1720mA ;
DDR2 2 Rnaks/8 pcs: 2350mA;
DDR_VTT: 300mA;
+1.5VRUN: 4130mA;



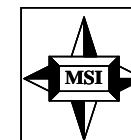
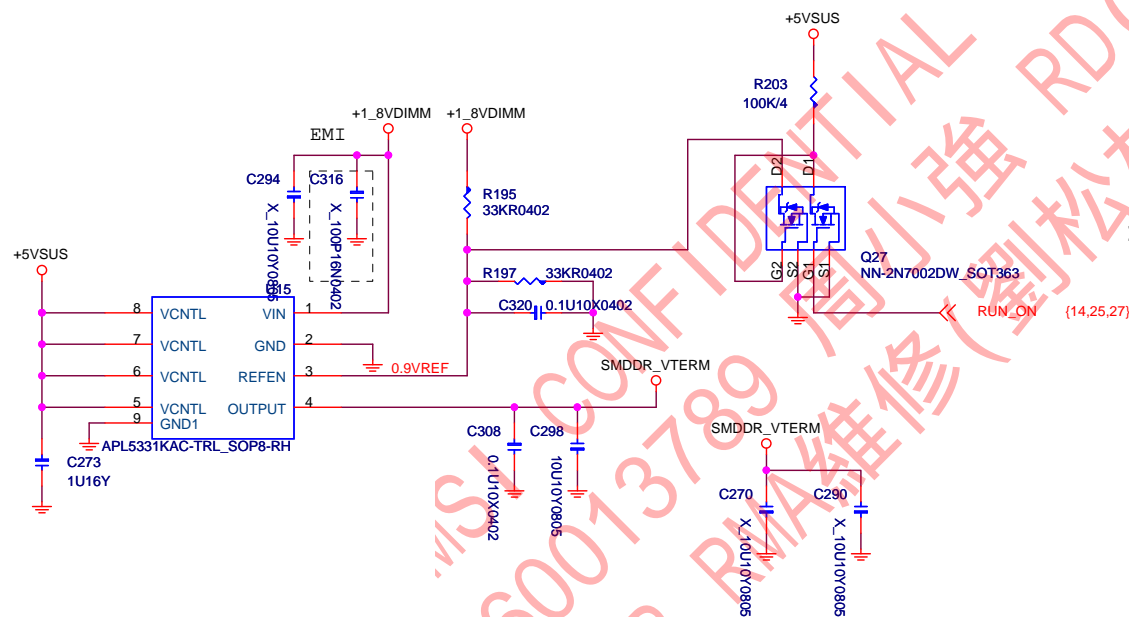
reserved for noise experiment

PWR_SRC

+1_8VDIMM

DDR_VTT 0.9V

DDR_VTT: 300mA;



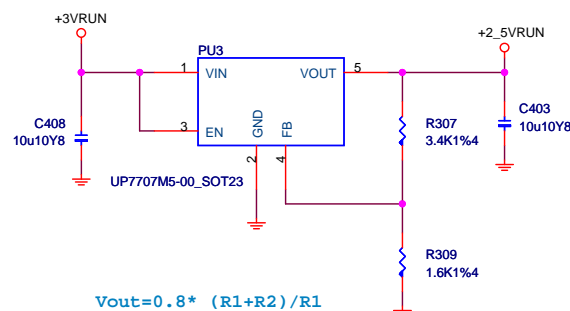
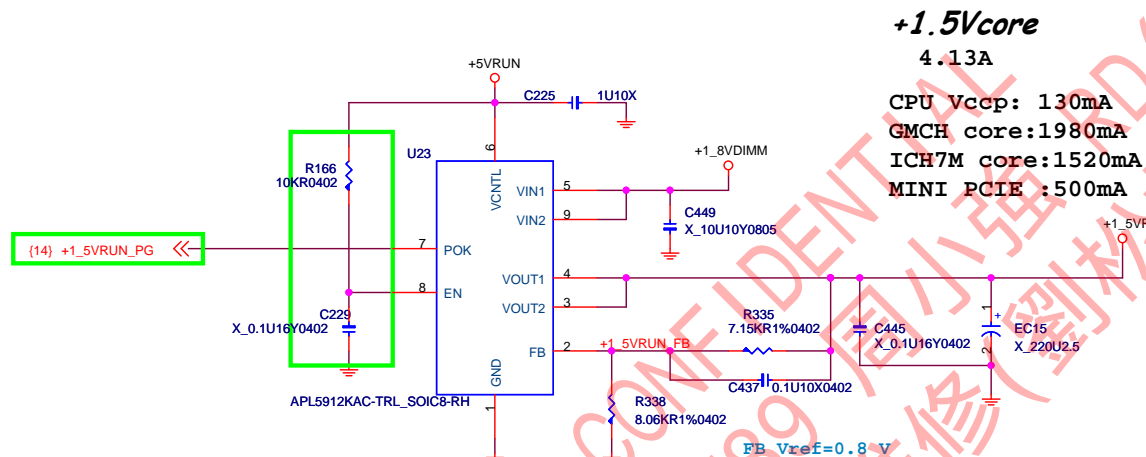
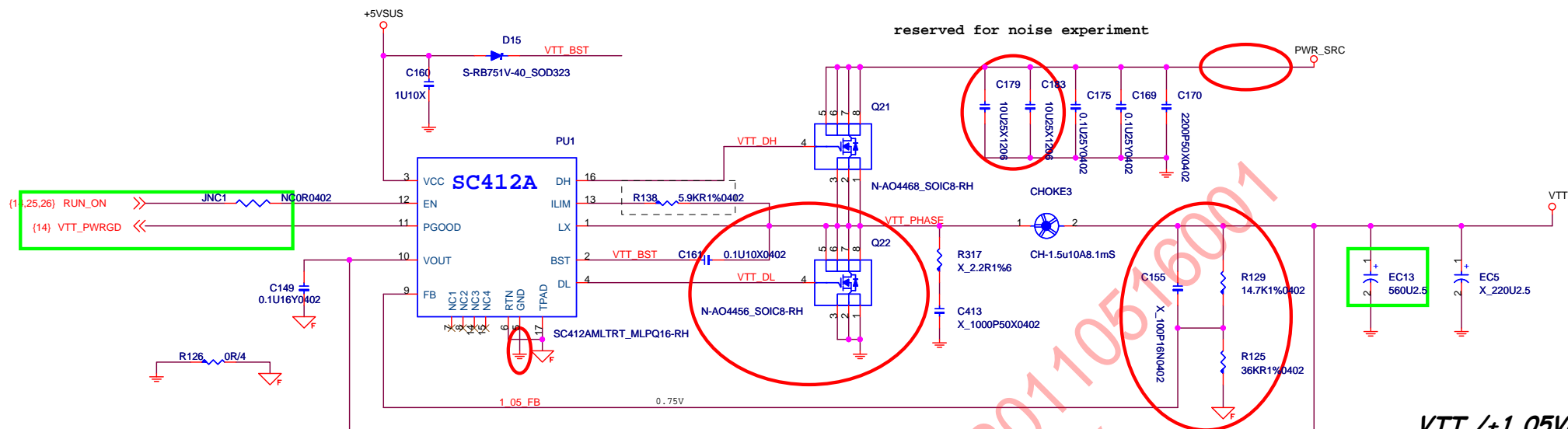
MICRO-STAR INT'L CO.,LTD

MS-N033

Size	Document Description	Rev
Custom	DDR & VTT_DDR Power	0A

Date: Thursday, November 13, 2008

Sheet 26 of 37



MICRO-STAR INT'L CO.,LTD

MS-N033

Size B

Document Description

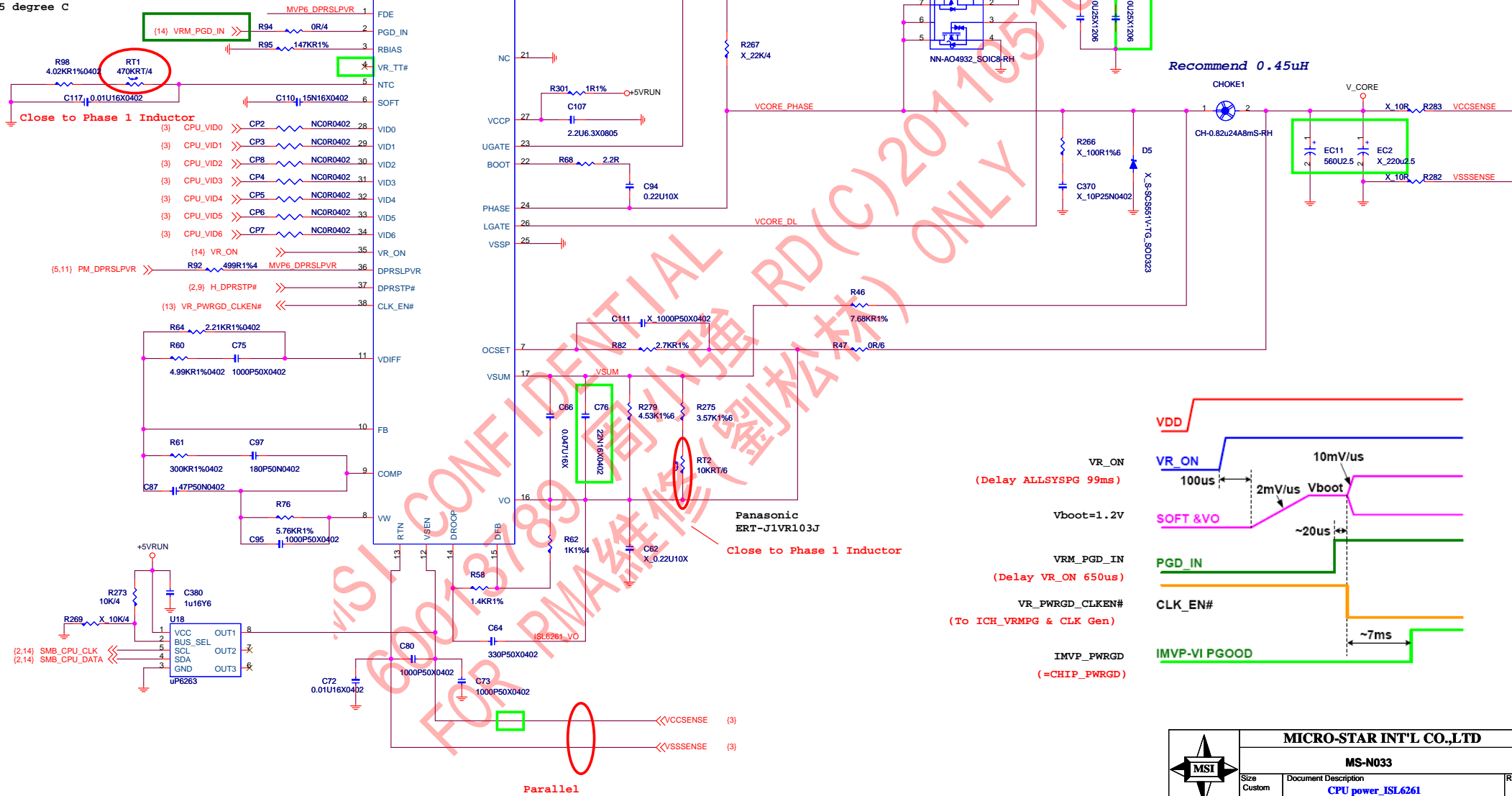
1.05V, 1.5V, 2.5V- POWER

Rev 0A

Date: Thursday, November 13, 2008

Sheet 27 of 37

VRM_PGD_IN rise after VR_ON 650us
Throttling temp.
105 degree C



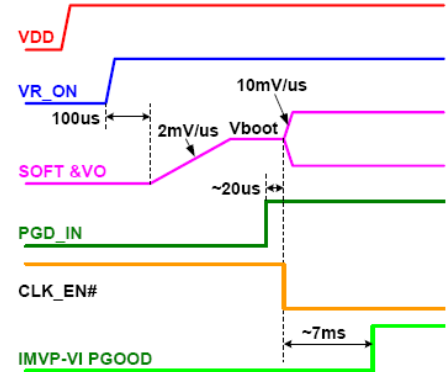
VR_ON
(Delay ALLSYSPG 99ms)

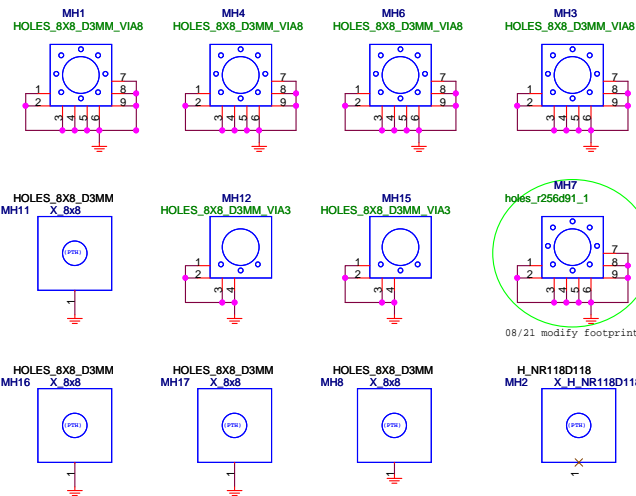
Vboot=1.2V

VRM_PGD_IN
(Delay VR_ON 650us)

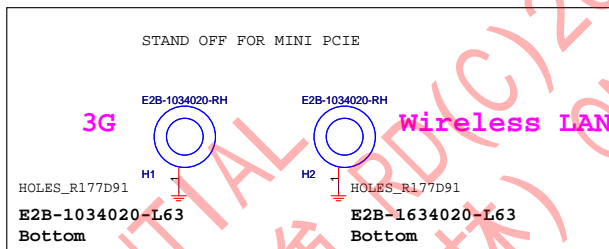
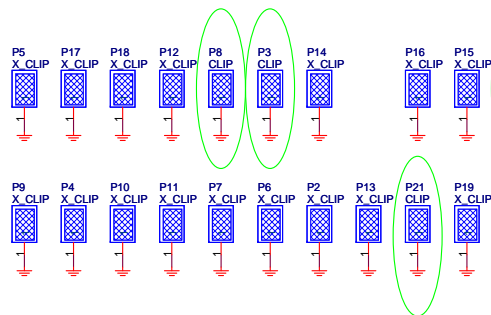
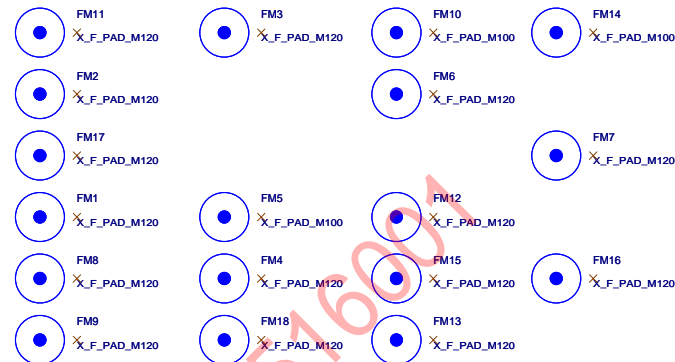
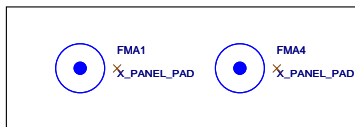
VR_PWRGD_CLKEN#
(To ICH_VRM PG & CLK Gen)

IMVP_PWRGD
(=CHIP_PWRGD)





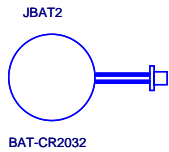
08/21 modify footprint in V1.0



Simulation

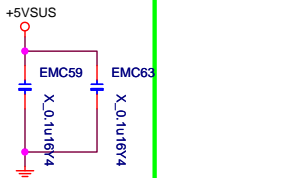
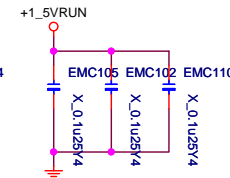
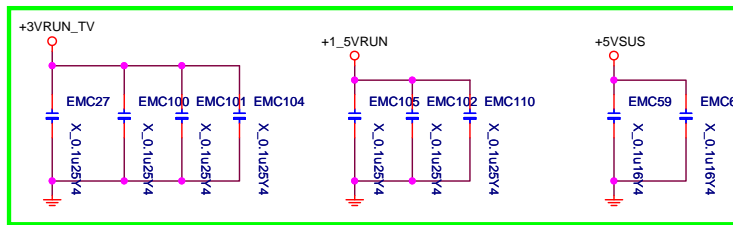
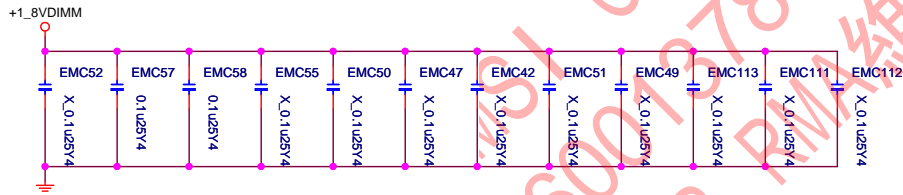
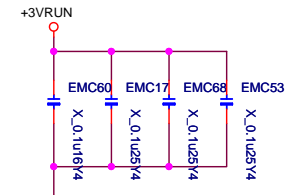
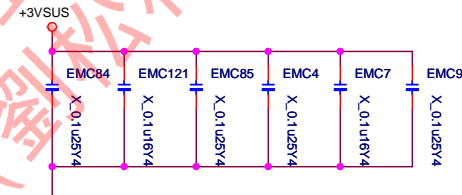
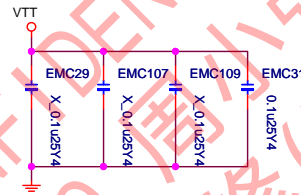
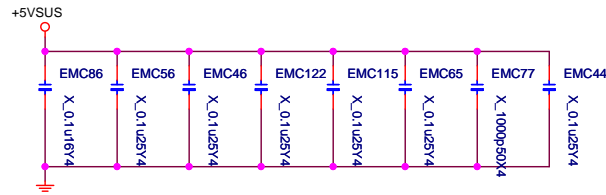
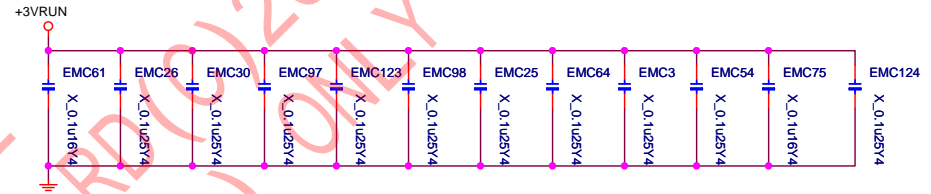
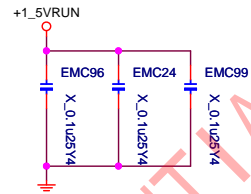
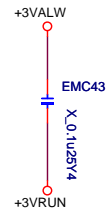
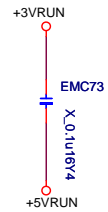
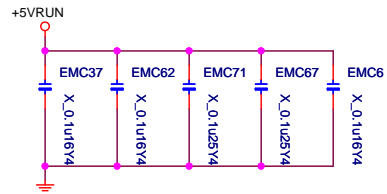
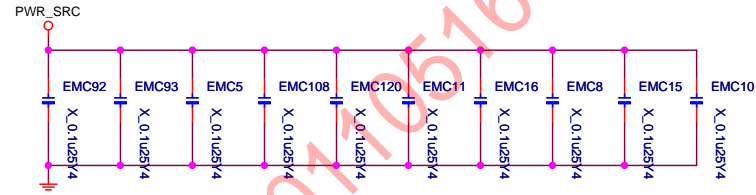
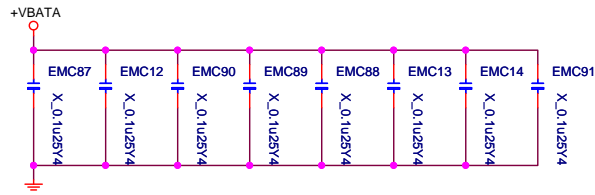
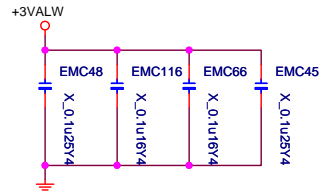
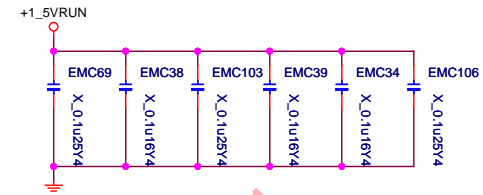
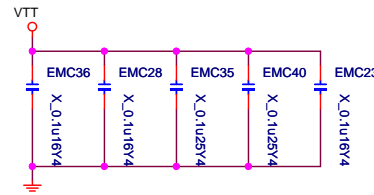


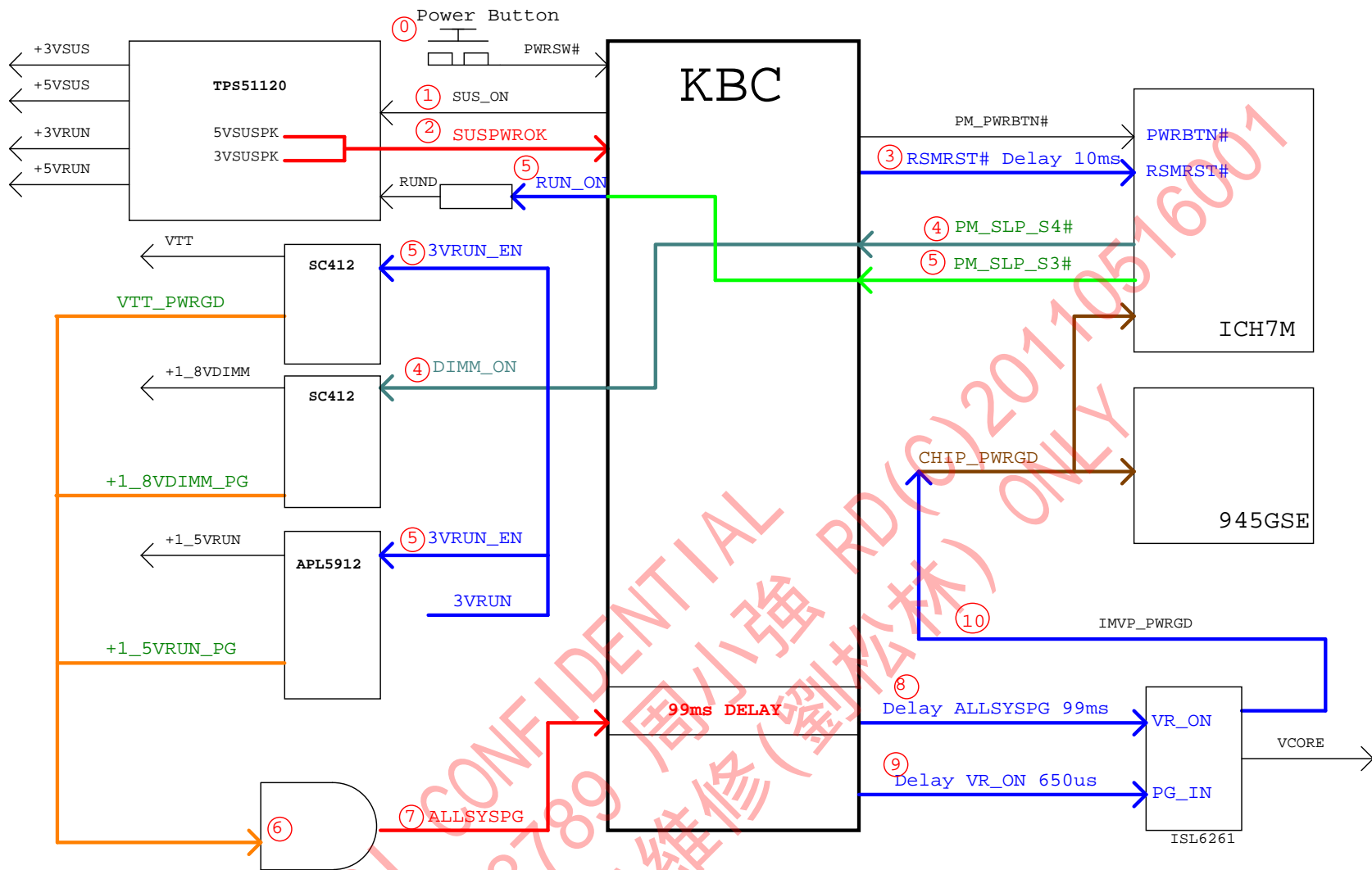
MICRO-STAR INT'L CO.,LTD			
MS-N033			
Size	Document Description		Rev
Custom	Screw		0A
Date: Thursday, November 13, 2008		Sheet	29 of 37



P30-N03310A-H73/D05

BIOS LABEL
G51-LA01678-A09
8/26 add in 1.0 BOM.

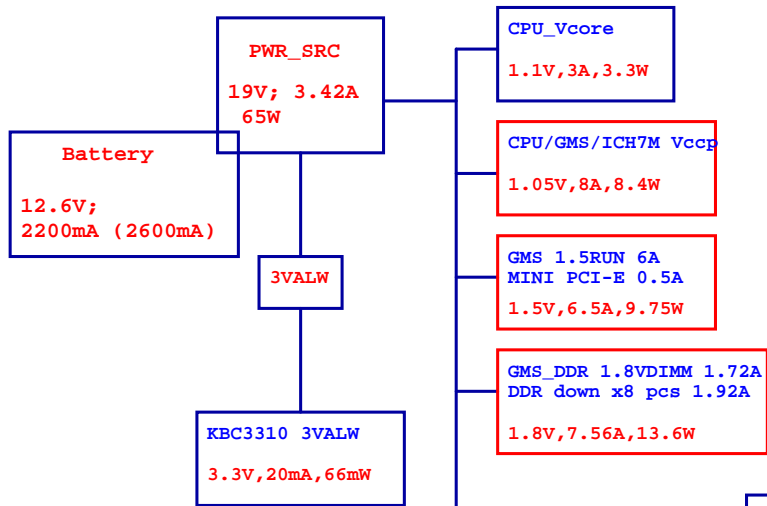




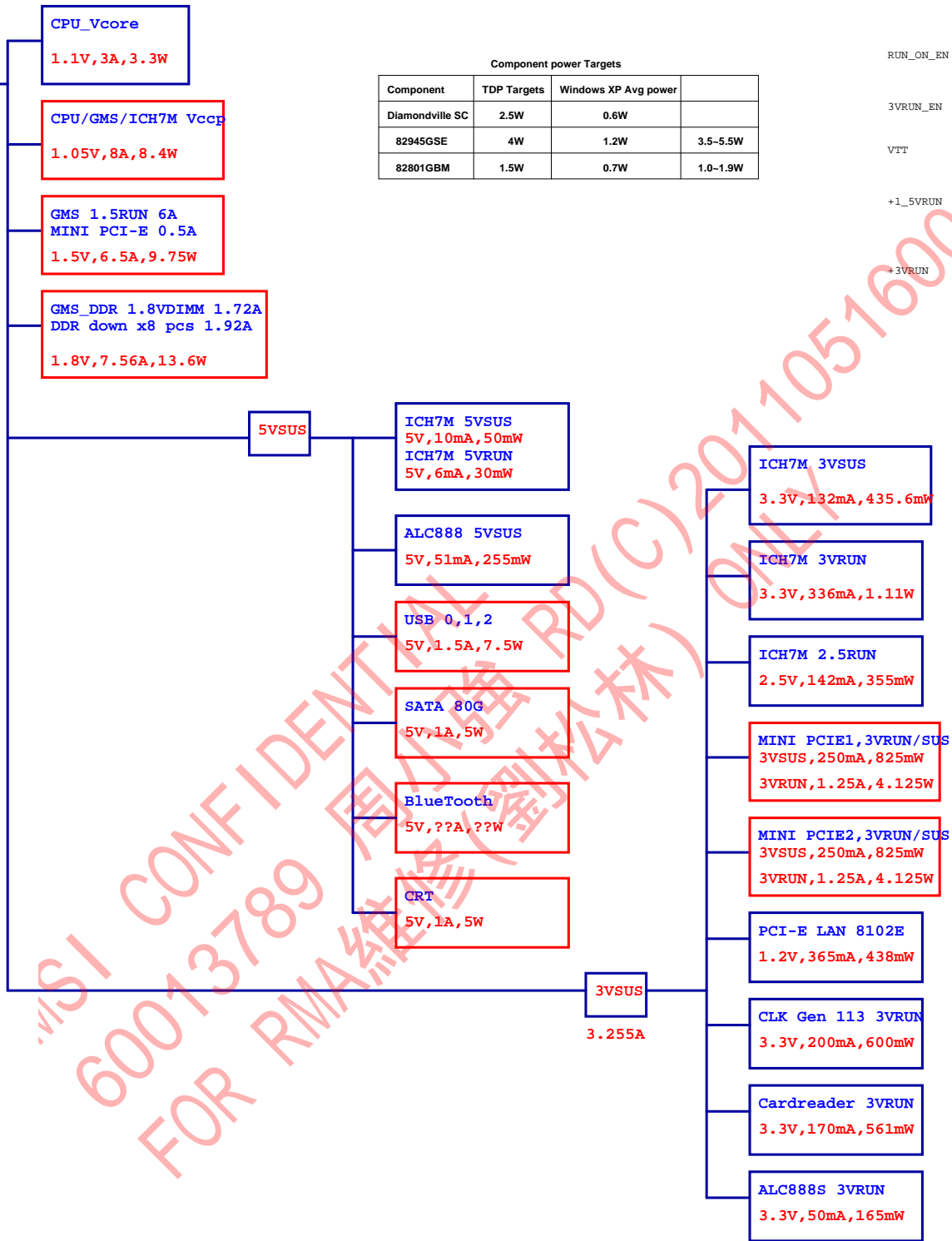
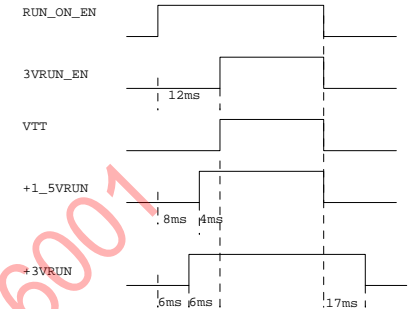
MICRO-STAR INT'L CO.,LTD

MS-N033

Size B	Document Description KBC_CTR_PWR_BD	Rev 0A
Date: Thursday, November 13, 2008	Sheet 31 of 37	

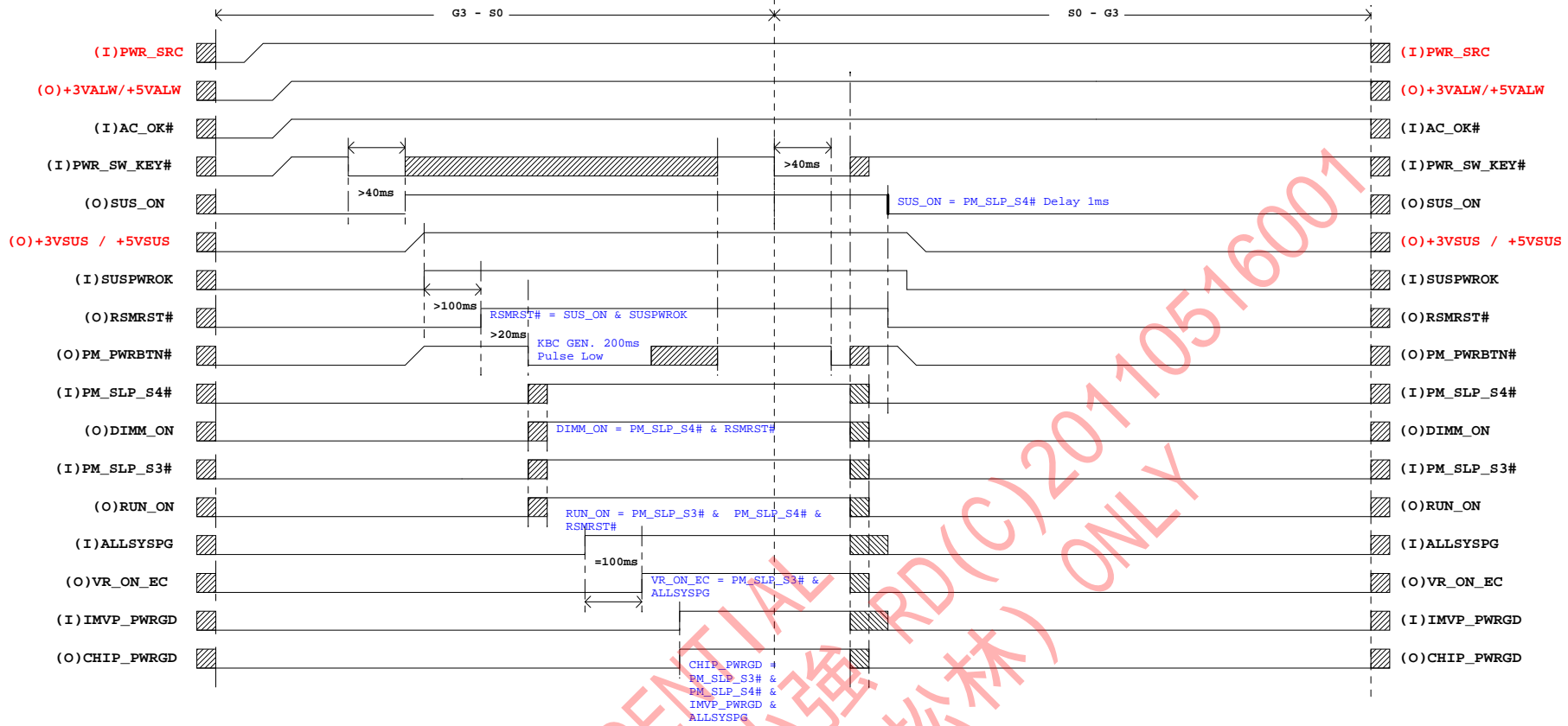


Component power Targets			
Component	TDP Targets	Windows XP Avg power	
Diamondville SC	2.5W	0.6W	
82945GSE	4W	1.2W	3.5-5.5W
82801GBM	1.5W	0.7W	1.0-1.9W



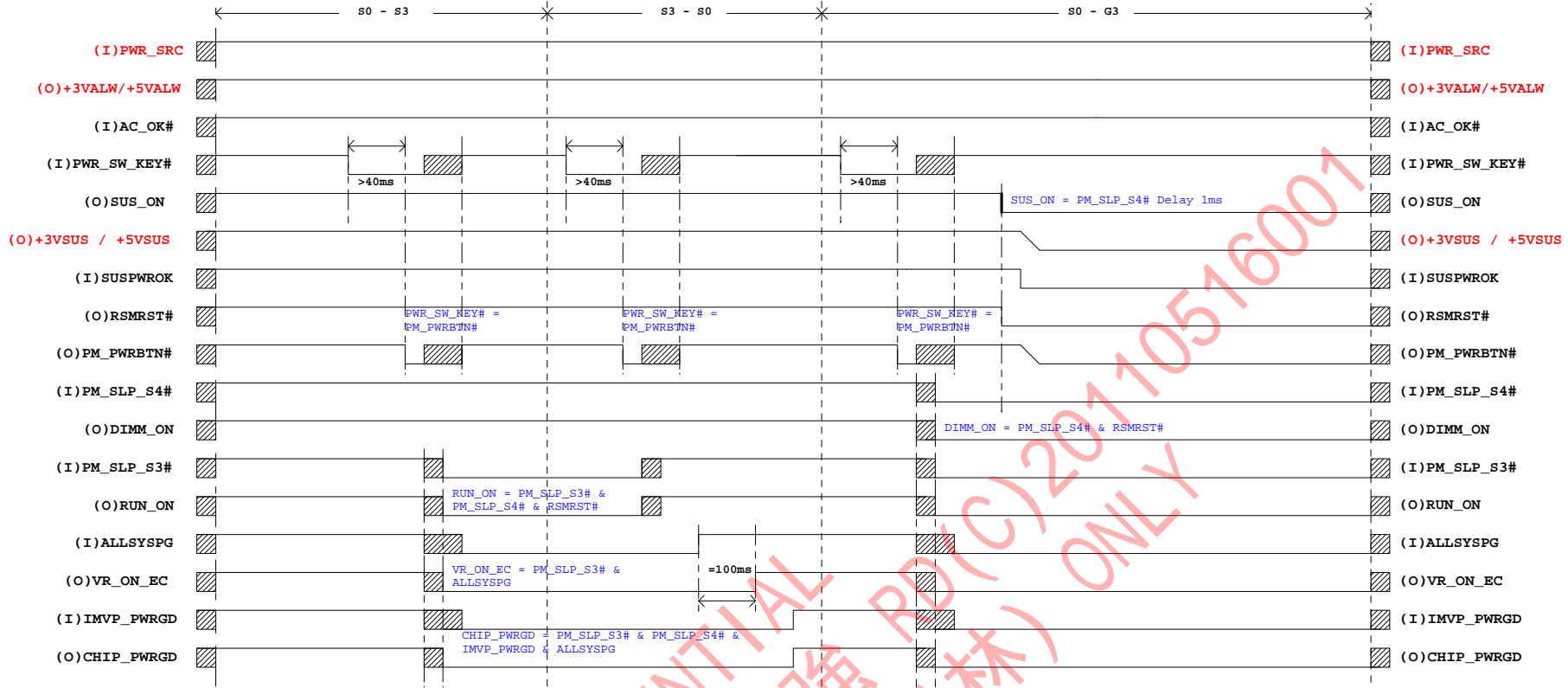
RED:POWER
BLACK:KBC

Battery Mode G3 - S0 - G3



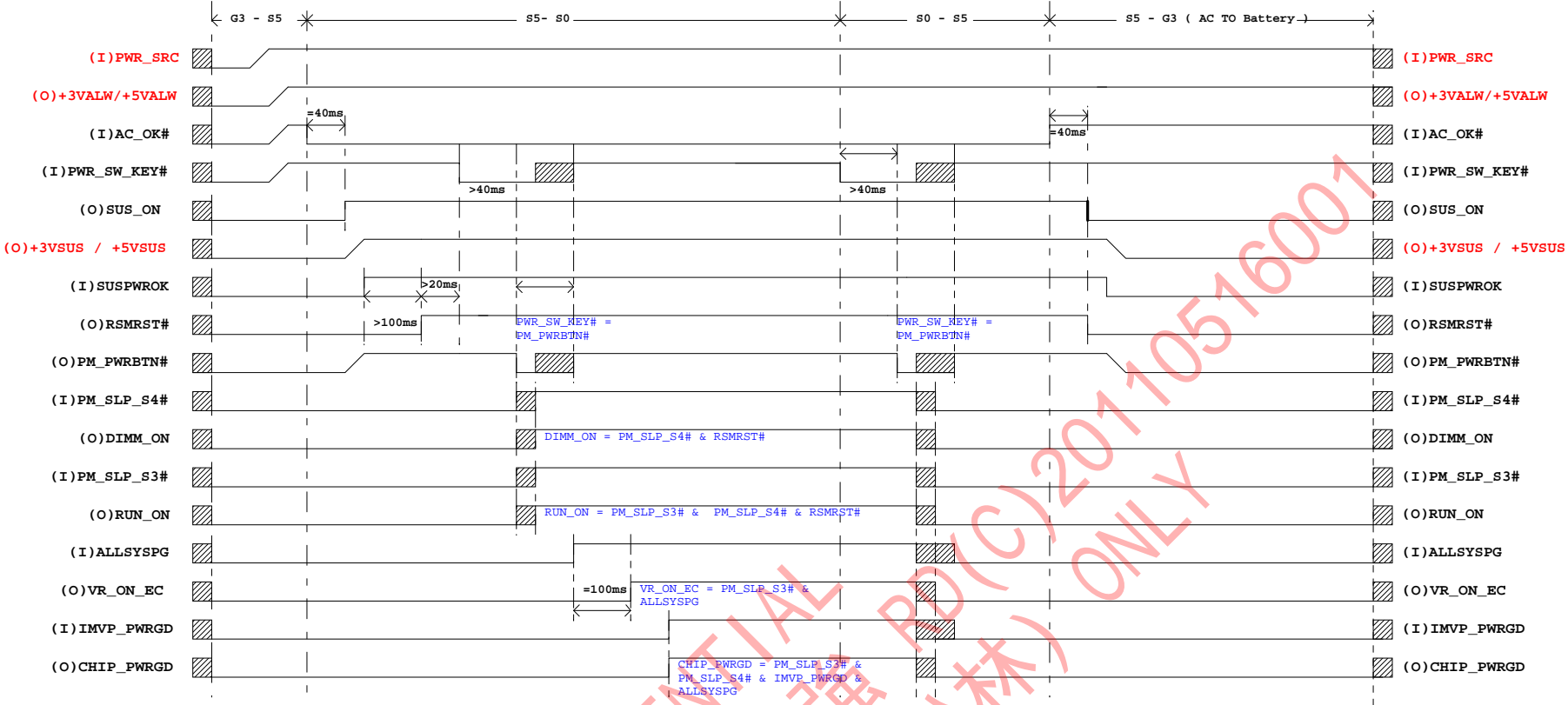
RED:POWER
BLACK:KBC

Battery Mode S0 - S3 - S0



RED: POWER
BLACK: KBC

AC Mode G3 - S5 - S0 - S5 - G3



RED: POWER
BLACK: KBC

AC Mode S0 - S3 - S0

